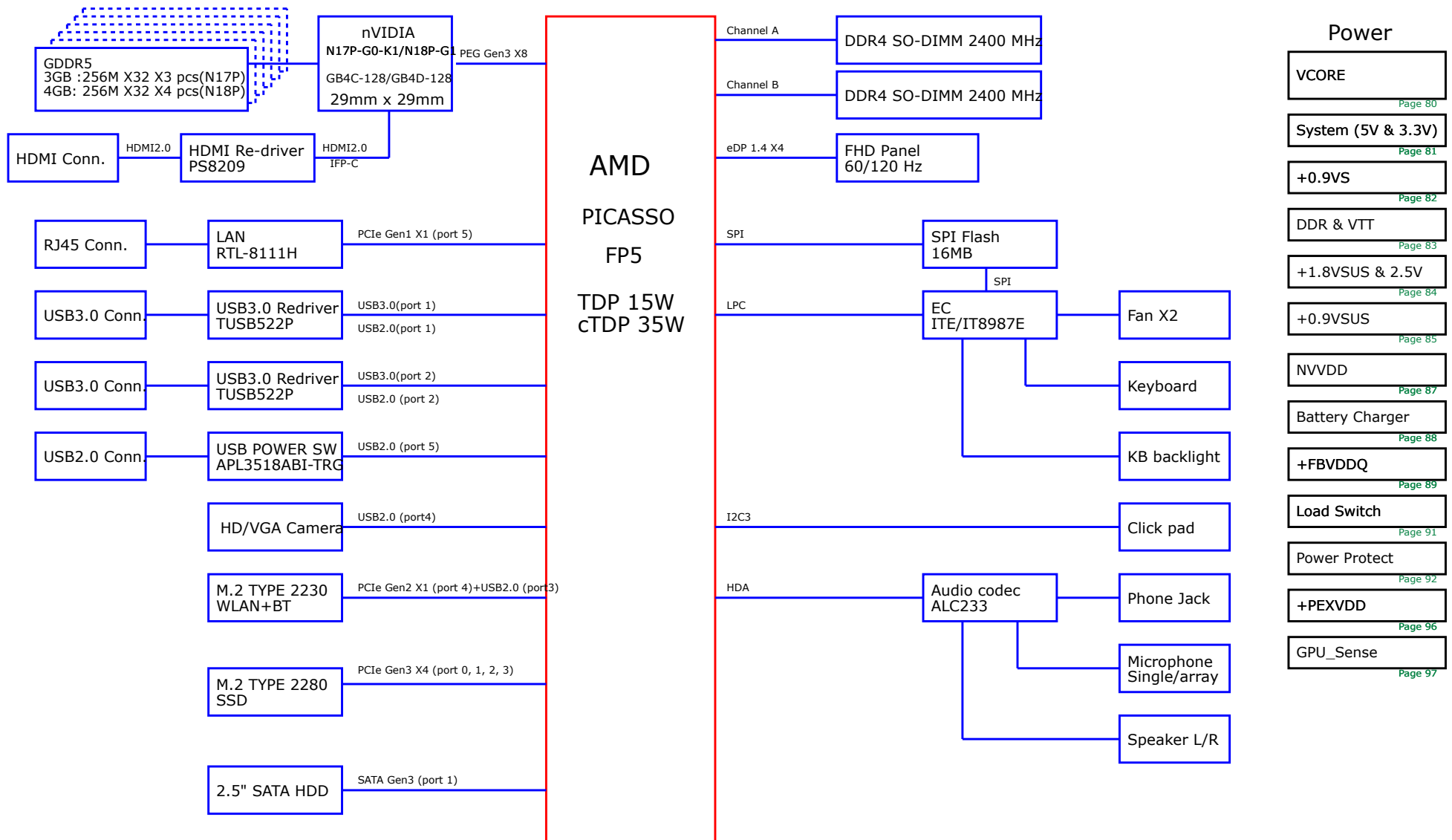
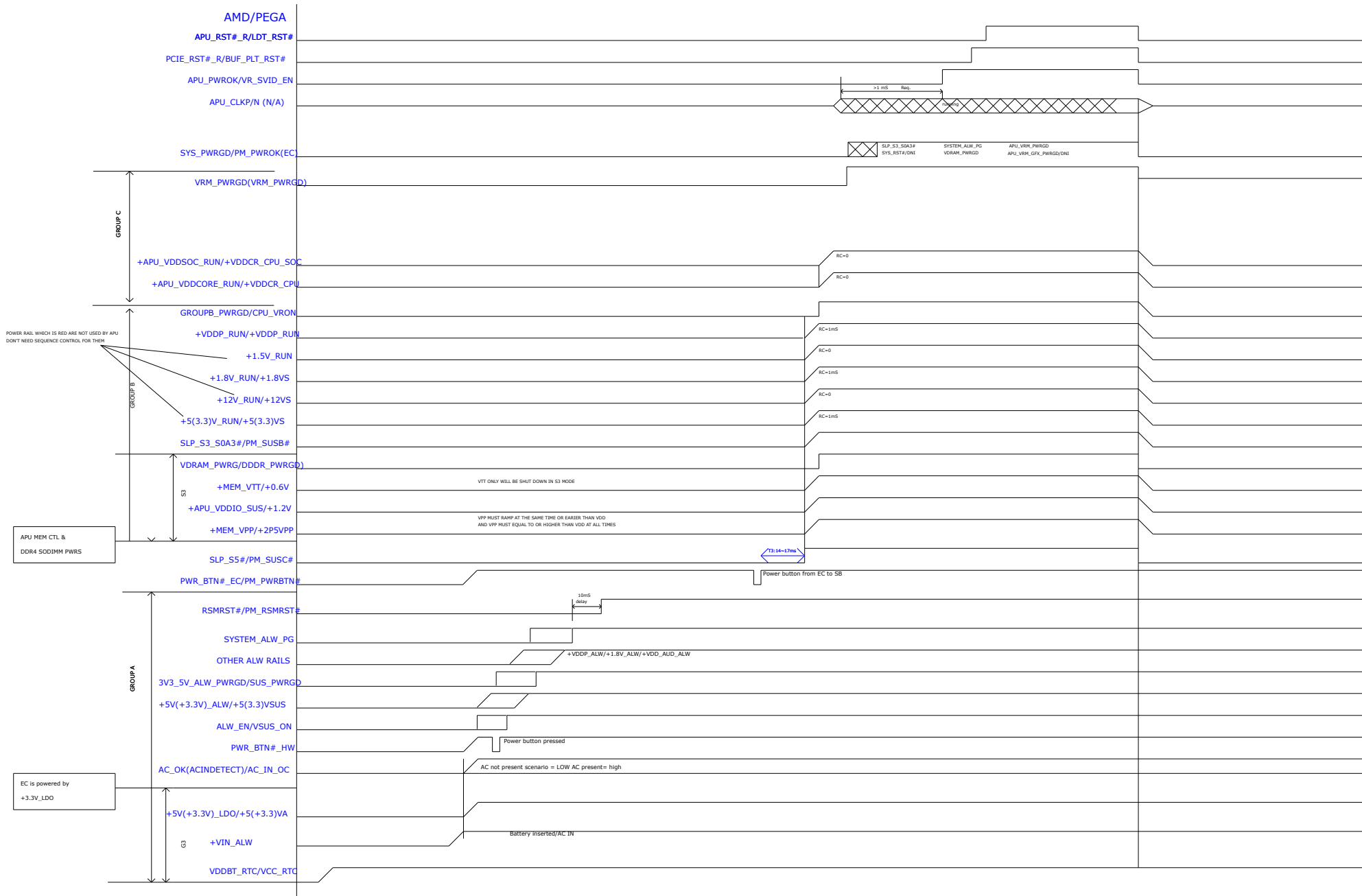


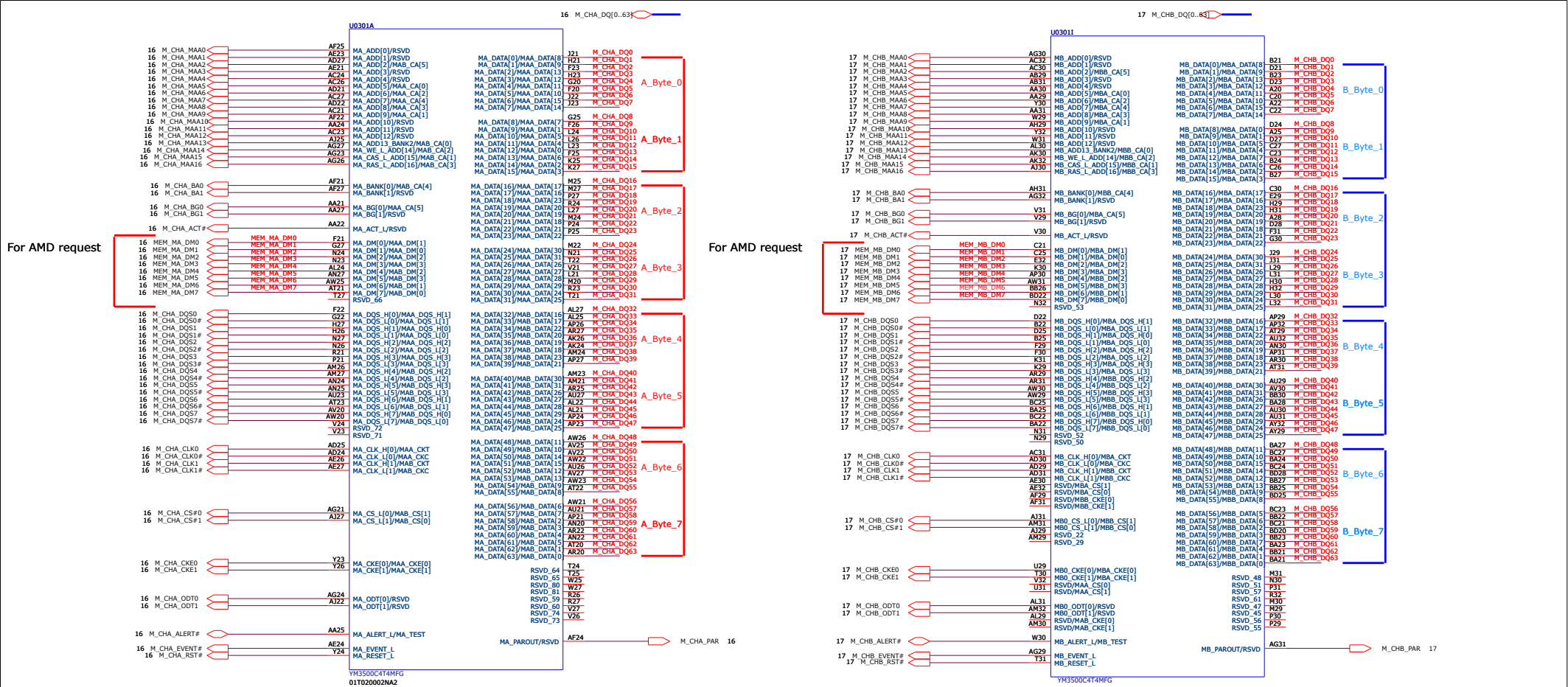
# FX505DD/DT Block Diagram



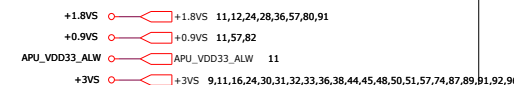
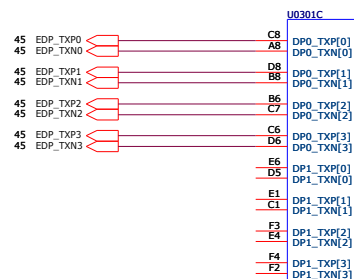






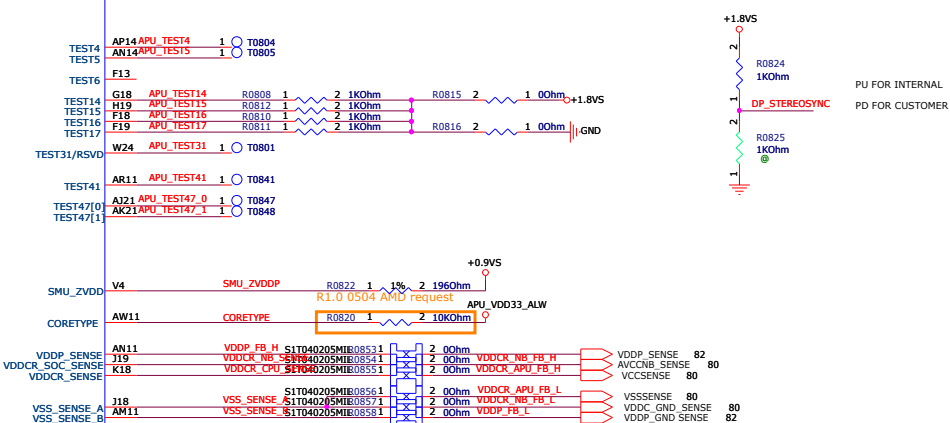




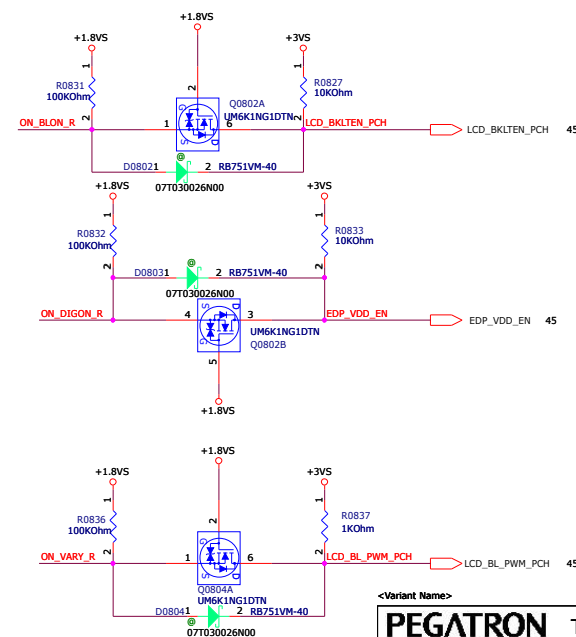


### 17.1.5 Power-Up Power Supply and Signal Sequencing

1. If the JTAG interface is used in a system, the TMS pin must be asserted a minimum of 10 ns before PWR\_GOOD assertion and must be held in the high state a minimum of 10 ns after the assertion of PWR\_GOOD.
2. After PWR\_GOOD assertion, the SVC/SVD signals change from the Boot VID to the value programmed during device manufacturing and the appropriate protocol for the SVI interface.
3. RESET\_L must remain asserted a minimum of 1 ms after PWR\_GOOD assertion.

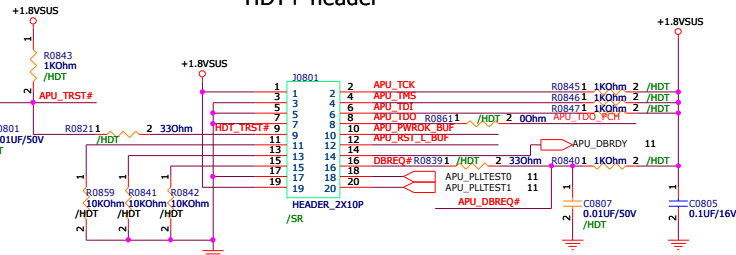


R0831, R0832, R0836 need to verify mount or un-mount for internal resistor

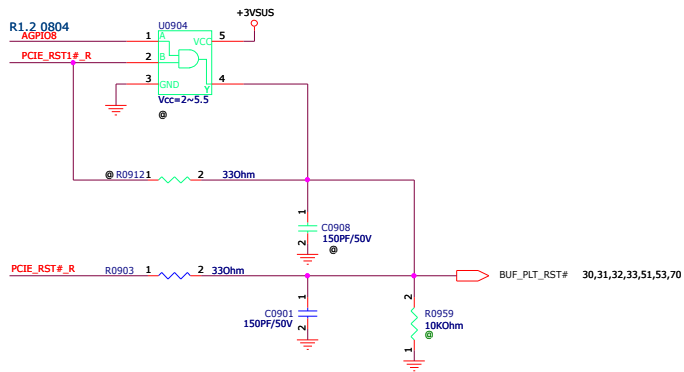


J0801 Only for EE Verify use

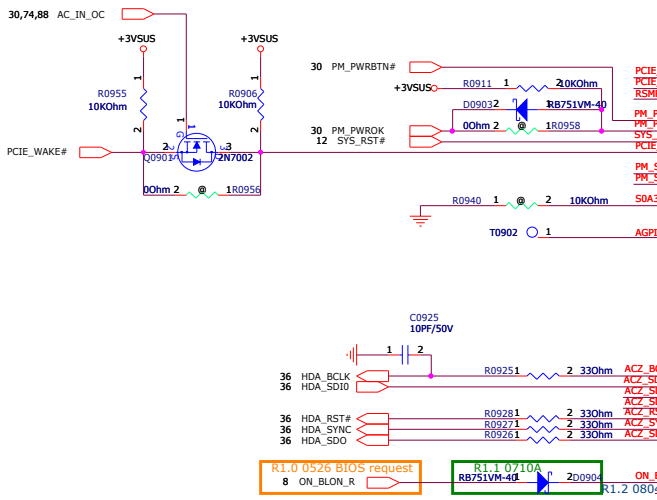
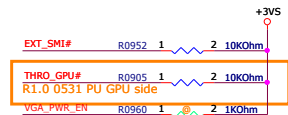
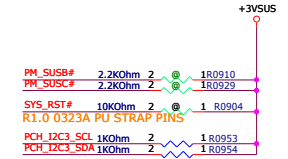
HDT+ header



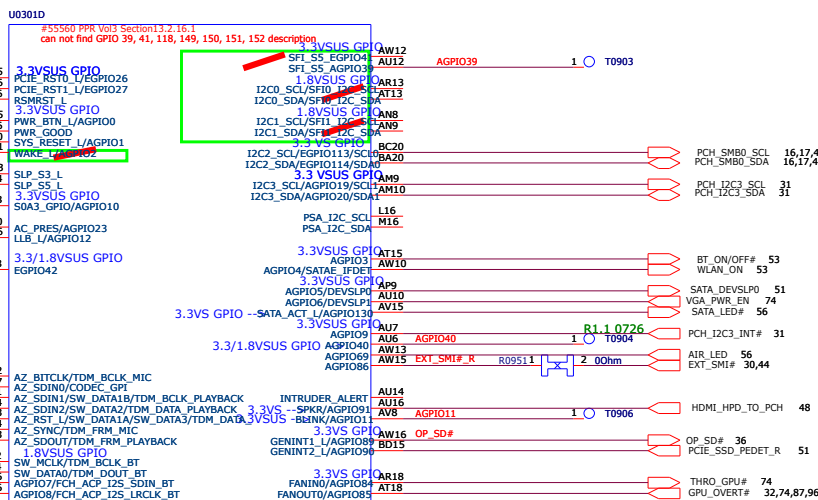
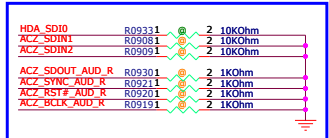




+1.8VSUS 1.8VSUS 8,11,12,24,28,36,57,80,91  
+3VS +3VS 8,11,16,24,30,31,32,33,36,38,44,45,48,50,51,57,74,87,89,91,92,96  
+3VSUS +3VSUS 11,12,23,24,30,31,33,36,42,51,53,74,81,88,92,96



#### HDAudio



#### SATA SSD1

<Variant Name>

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Size C Project Name BK5EA Engineer: Jack Lee

Date: Tuesday, March 12, 2019 Sheet 9 of 72

Rev 1.1





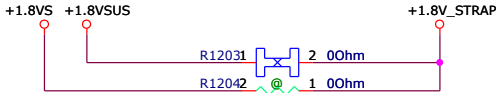


- +1.8VSUS
- +1.8VS
- +3VSUS
- +1.8VSUS

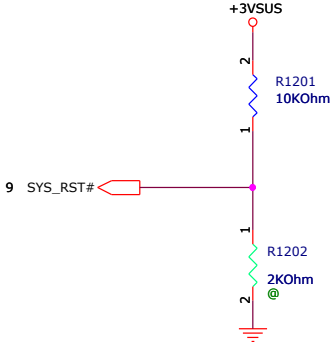
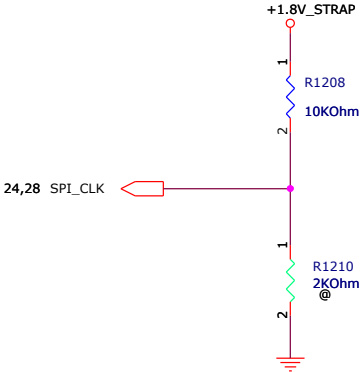
8,9,11,24,28,53,80,84
- +1.8VS

8,11,24,28,36,57,80,91
- +3VSUS

9,11,23,24,30,31,33,36,42,51,53,74,81,88,92,96



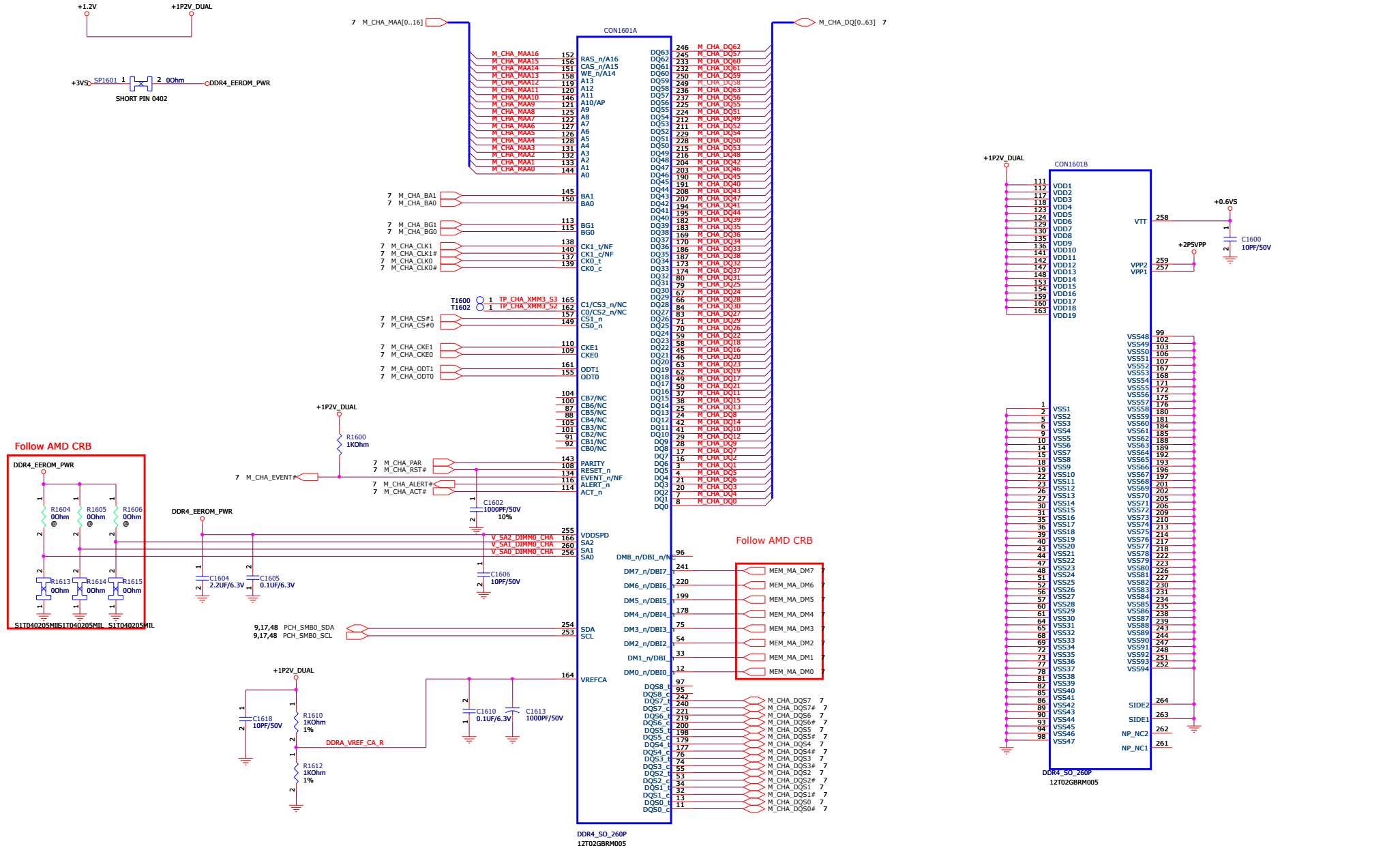
STRAP PINS



STRAP	FUNCTION	DEFINITION
SPI_CLK		1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#		1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

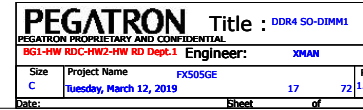


# DDR4 SO-DIMM 5.2H REV





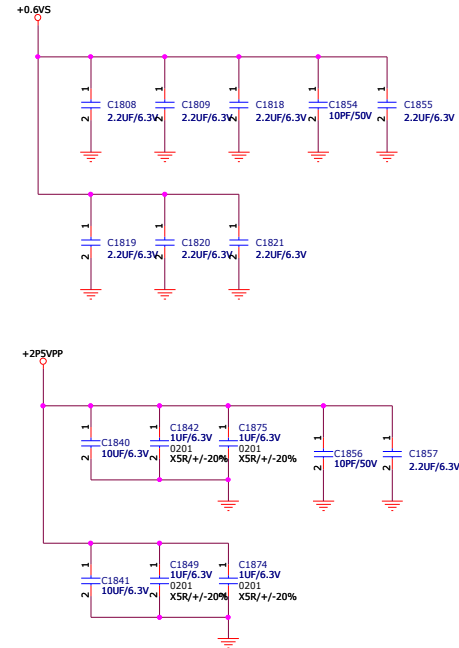
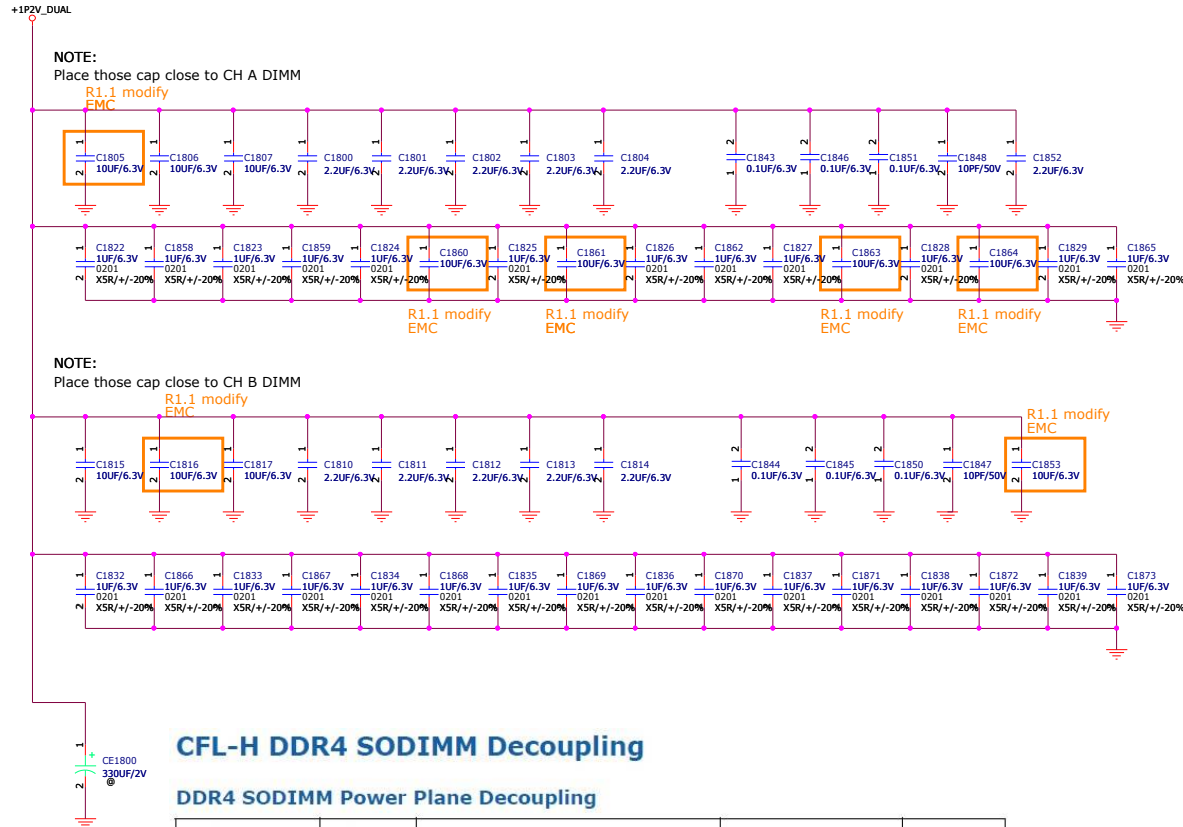
+1.2V	○	○	+1.2V	11,16,18,57,83
+1P2V_DUAL	○	○	+1P2V_DUAL	11,16,18,57,83
+0.6VS	○	○	+0.6VPS	16,18,57,83
+2P5VPP	○	○	+2P5VPP	16,18,57,84
+3VS	○	○	+3VS	8,9,11,16,24,30,31,32,33,36,38,44,45,48,50,51,57,74,87,89,91,92,96





+1.2V  
 +1P2V\_DUAL  
 +0.6VS  
 +2P5VPP  
 +3VS

+1.2V 11,16,17,57,83  
 +1P2V\_DUAL 11,16,17,57,83  
 +0.6VS 16,17,57,83  
 +2P5VPP 16,17,57,84  
 +3VS 8,9,11,16,24,30,31,32,33,36,38,44,45,48,50,51,57,74,87,89,91,92,96



## CFL-H DDR4 SODIMM Decoupling

### DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x $\mu$ F (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 $\mu$ F (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1 $\mu$ F (0402)	
		1 placeholder	1x 330 $\mu$ F (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10 $\mu$ F (0603)	
		Placed on VTT plane close to DIMM	4x 1 $\mu$ F (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10 $\mu$ F (0603)	
		DIMM Pin side, 1 per DIMM	2x 1 $\mu$ F (0402)	
	VDDSPD	Place close to DIMM	2x 0.1 $\mu$ F (0402)	
		Place close to DIMM	2x 2.2 $\mu$ F (0402)	

**PEGATRON** Title : DDR4 Caps.

PEGATRON PROPRIETARY AND CONFIDENTIAL

BGI-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size Project Name FXS05GE

C Tuesday, March 12, 2019 18 Rev 72 1.0

Date: Sheet of

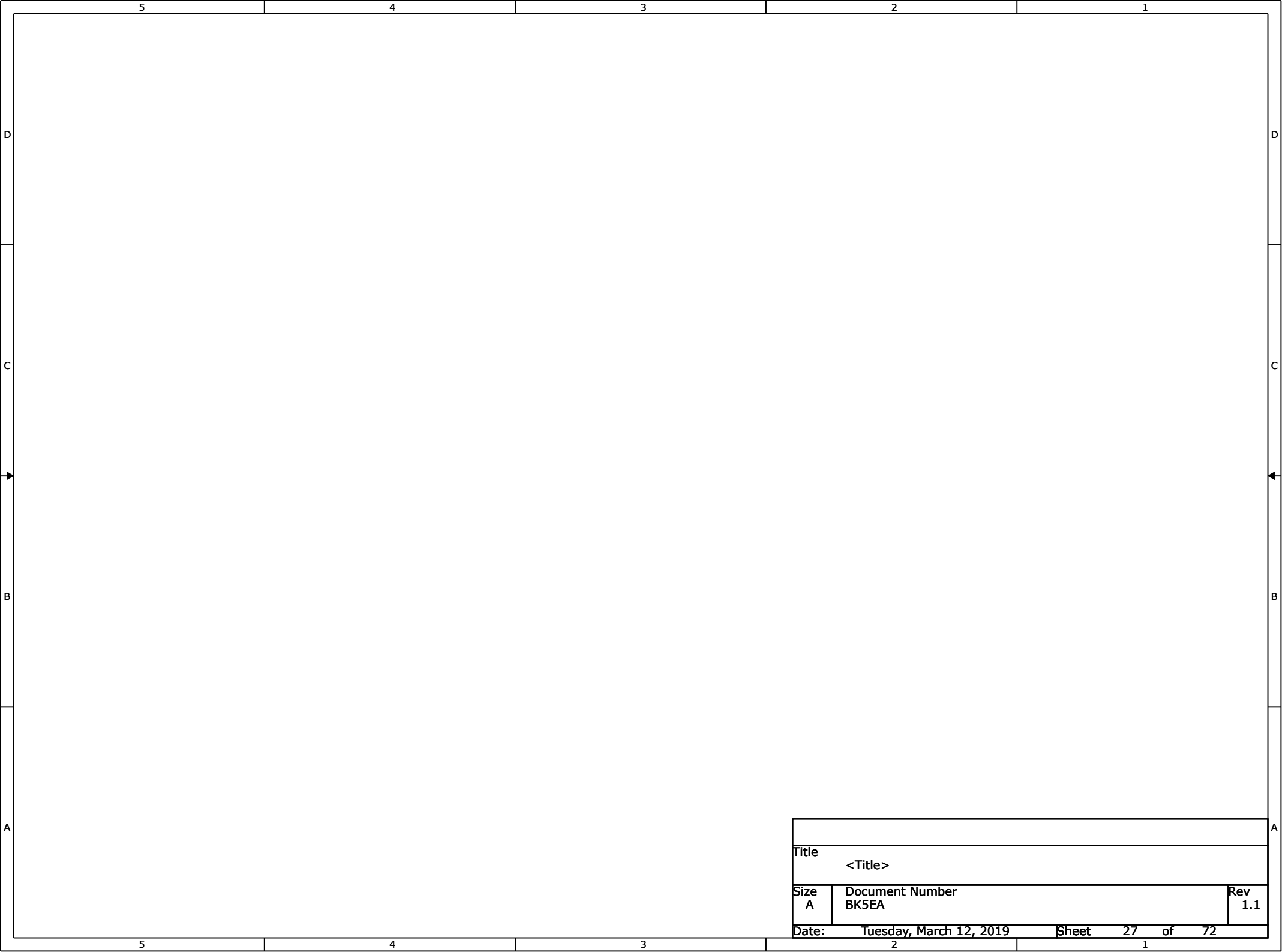






<b>PEGATRON</b> Title <b>PCH(5)_CLK</b> PEGATRON PROPRIETARY AND CONFIDENTIAL <b>BGI-HW3 RD</b> Engineer: <b>Jack_Lee</b>	
Size Custom	Project Name <b>BK5EA</b>
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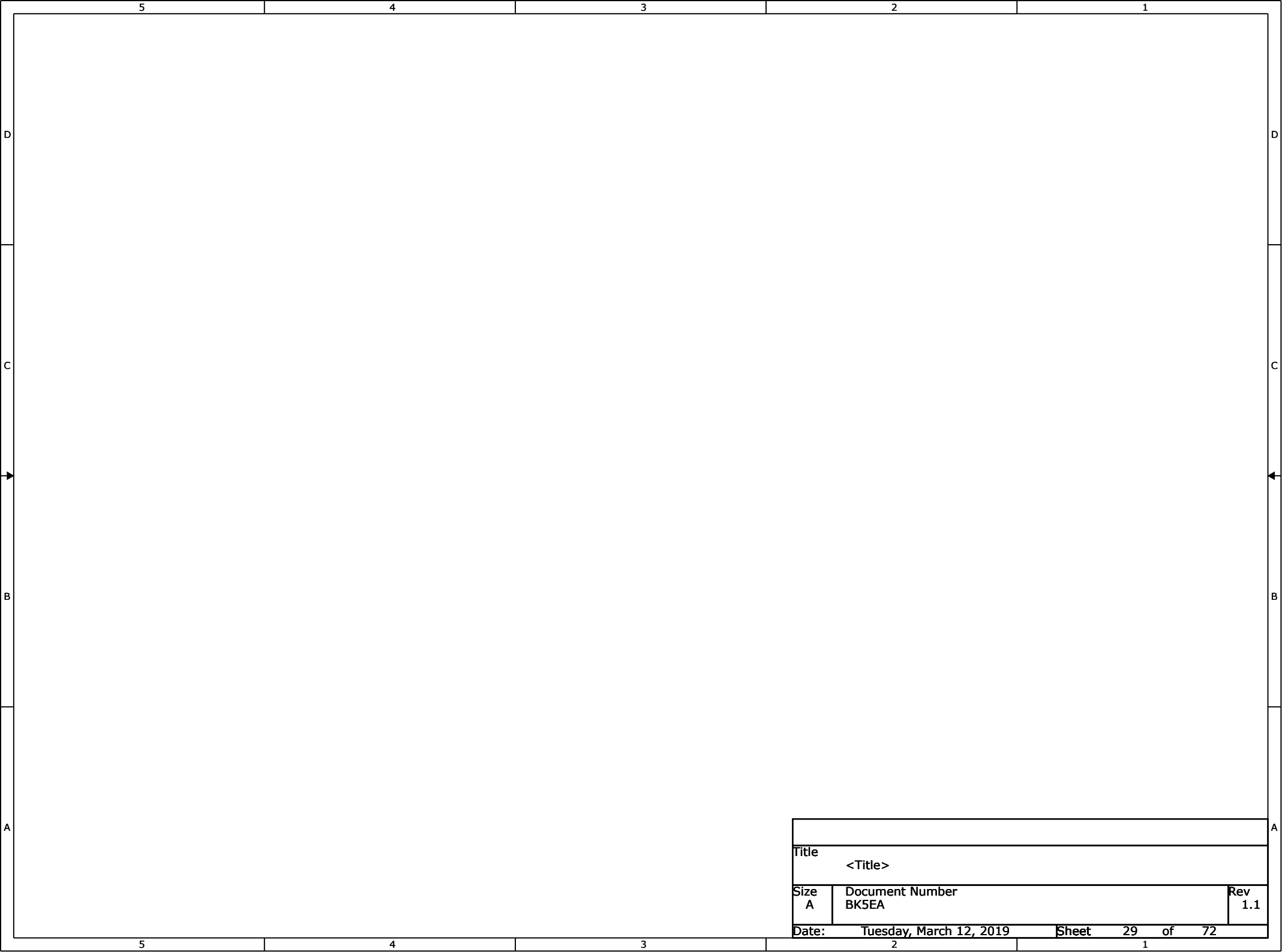


Title		
<Title>		
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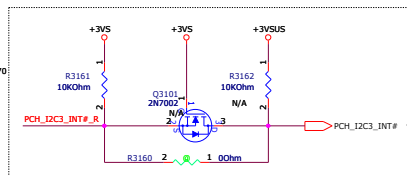
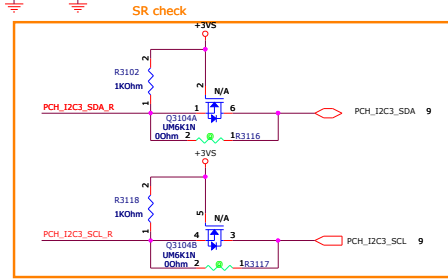
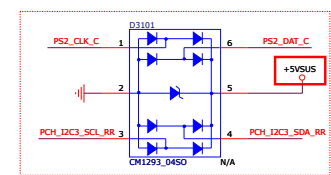
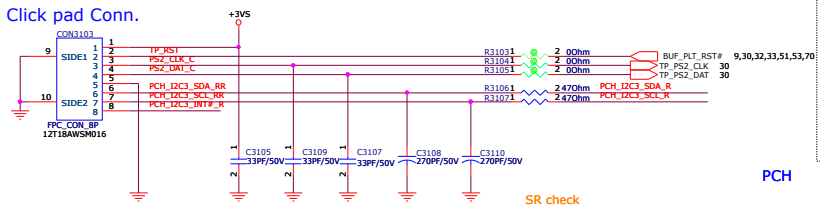




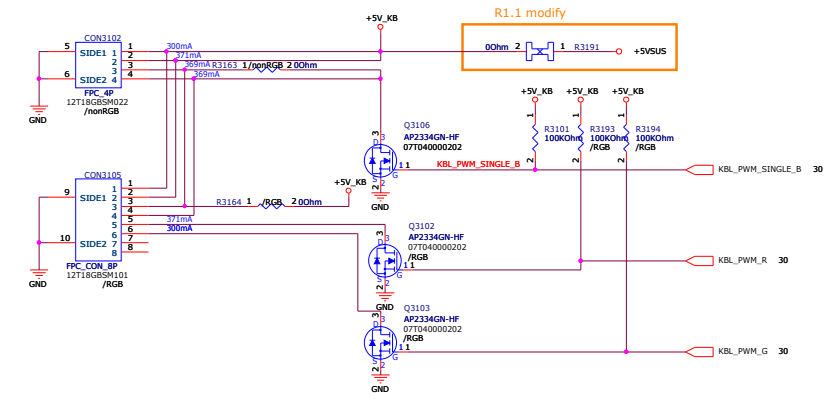




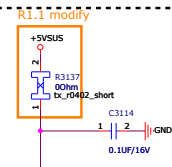
Click pad Conn.



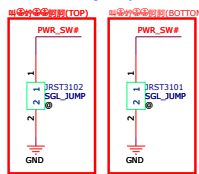
## KB Backlight Conn.



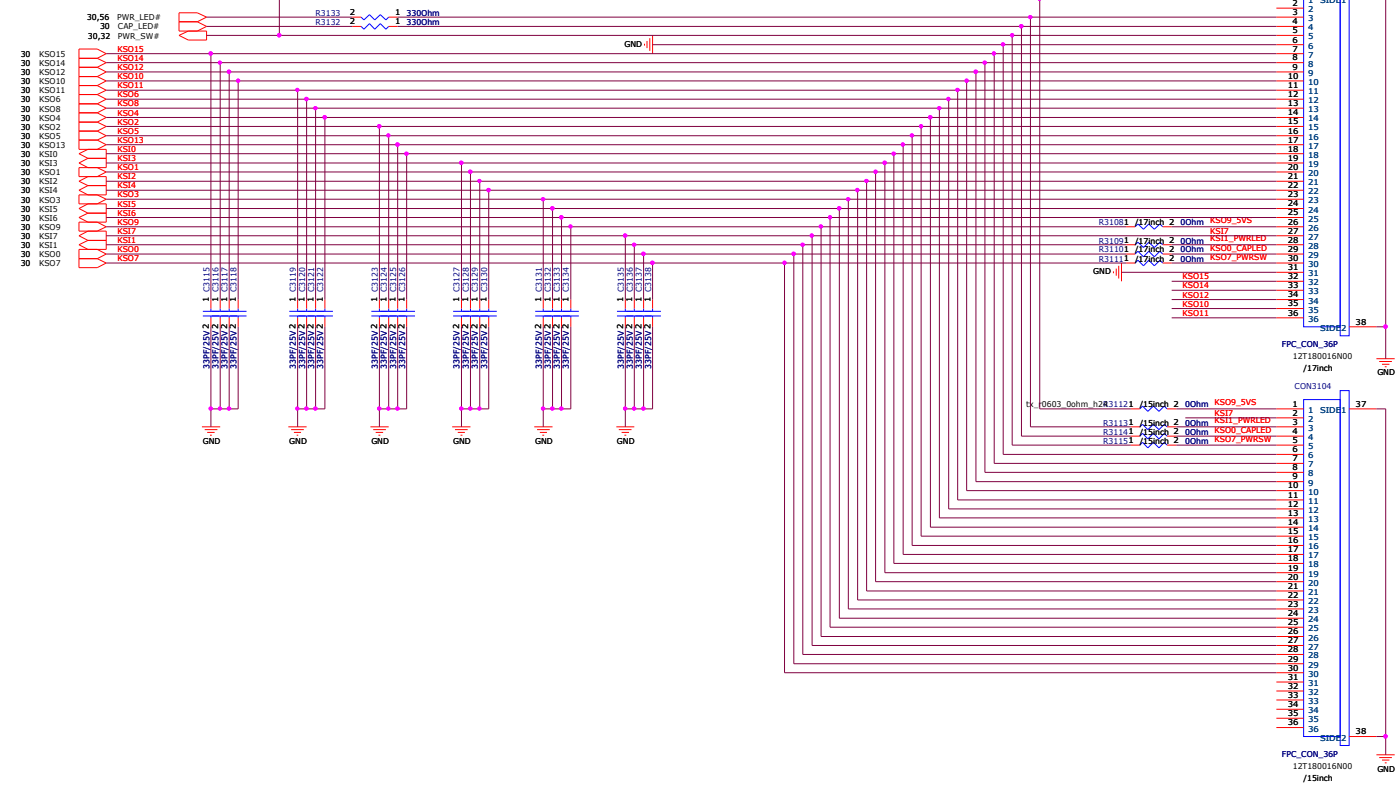
## Keyboard Conn.



## Power-on jumper

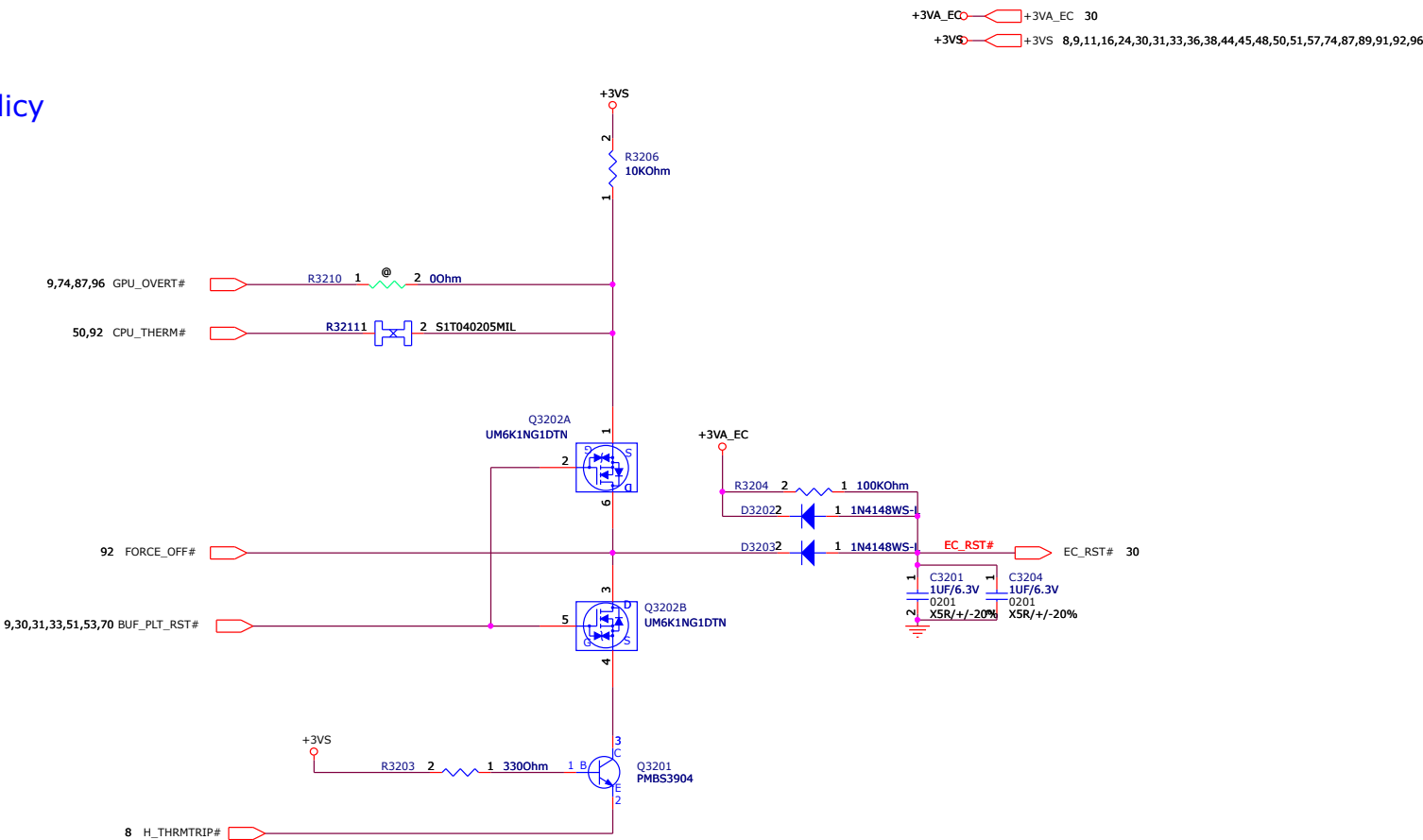


PN 1	LED VCC
PN 2	NC
PN 3	Power LED
PN 4	CapsLoad: NC
PN 5	Power SW
PN 6	Power GND
PN 7	KS015
PN 8	KS014
PN 9	KS012
PN 10	KS011
PN 11	KS010
PN 12	KS006
PN 13	KS008
PN 14	KS004
PN 15	KS002
PN 16	KS008
PN 17	KS013
PN 18	KS010
PN 19	KS013
PN 20	KS011
PN 21	KS012
PN 22	KS014
PN 23	KS003
PN 24	KS015
PN 25	KS016
PN 26	KS009
PN 27	KS017
PN 28	KS011
PN 29	KS000
PN 30	KS007
PN 31	NC
PN 32	NC
PN 33	NC
PN 34	NC
PN 35	NC
PN 36	NC

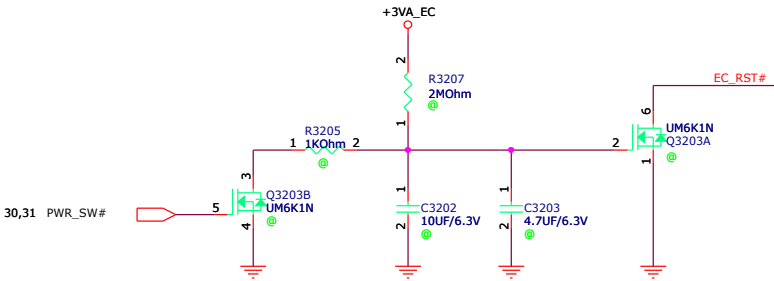




Thermal Policy

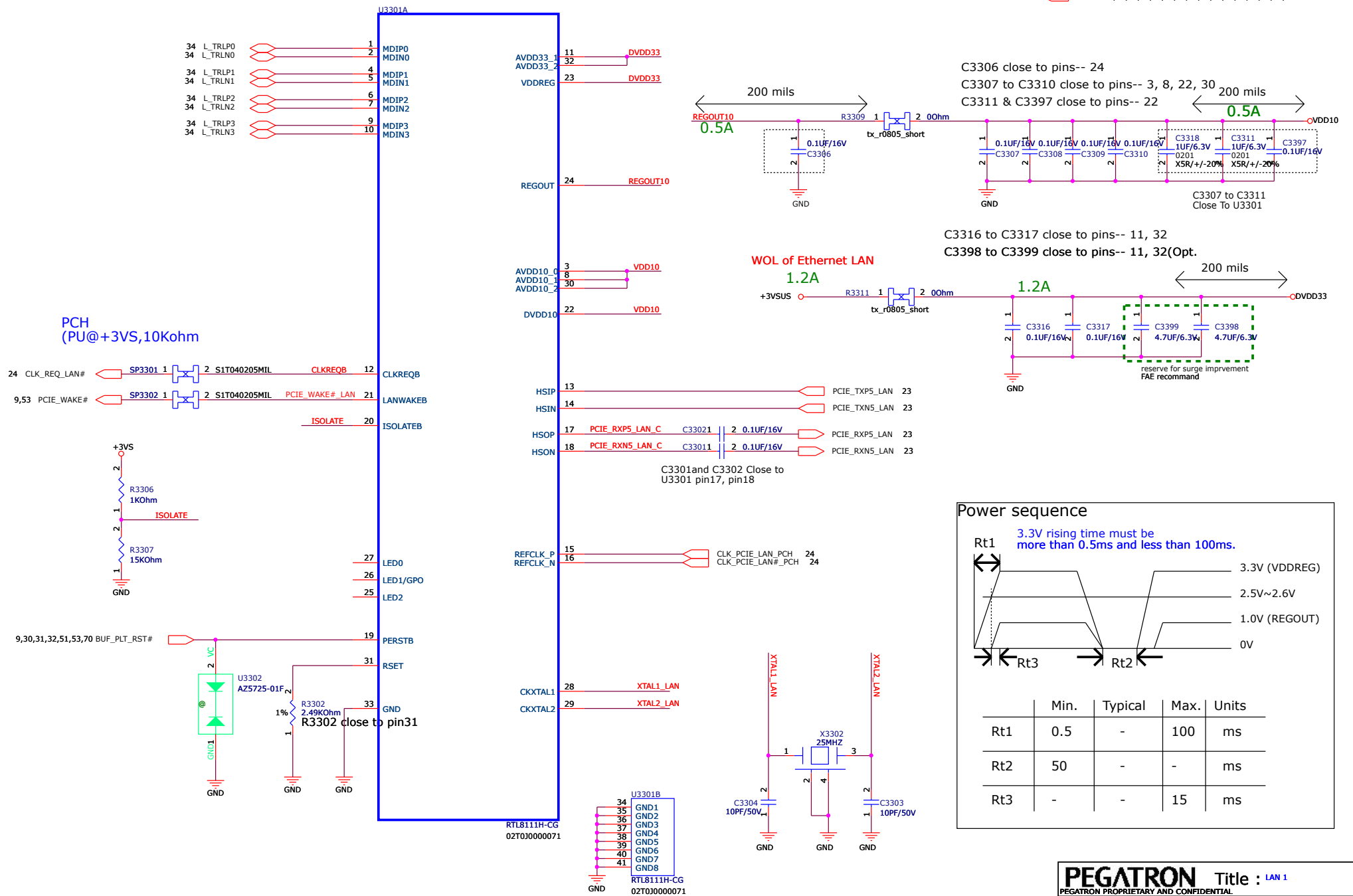


EC reset



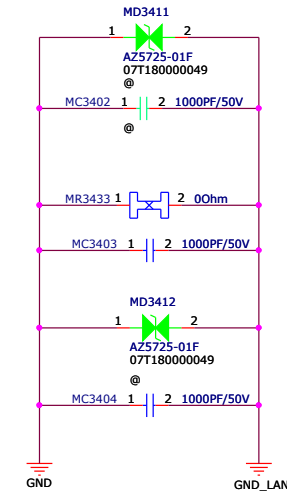
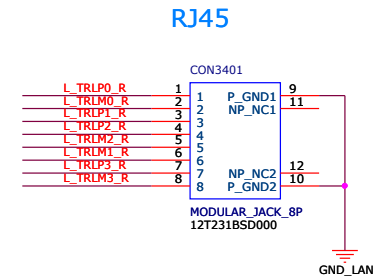
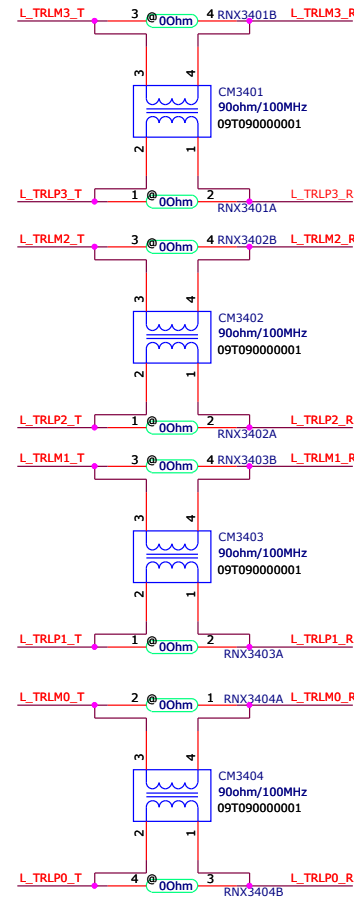
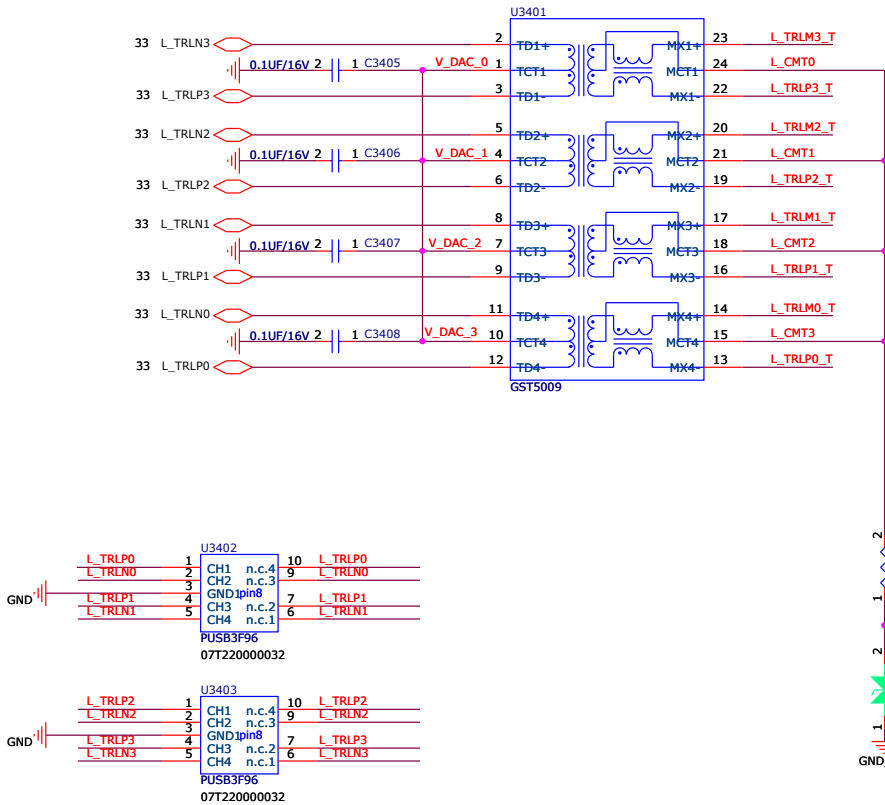
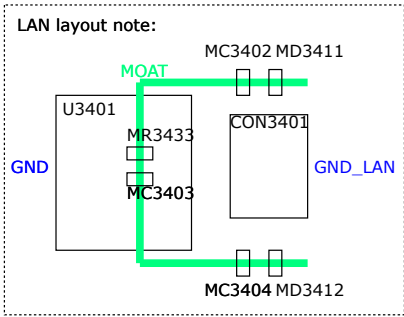


### 33.Realtek RTL8111H



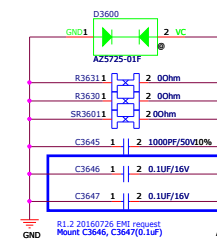
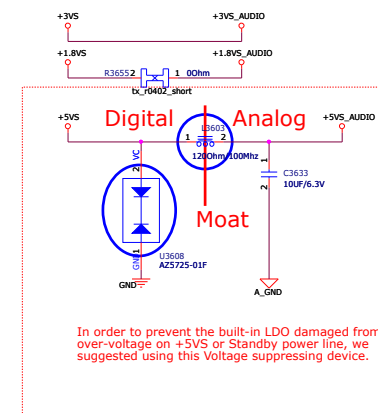
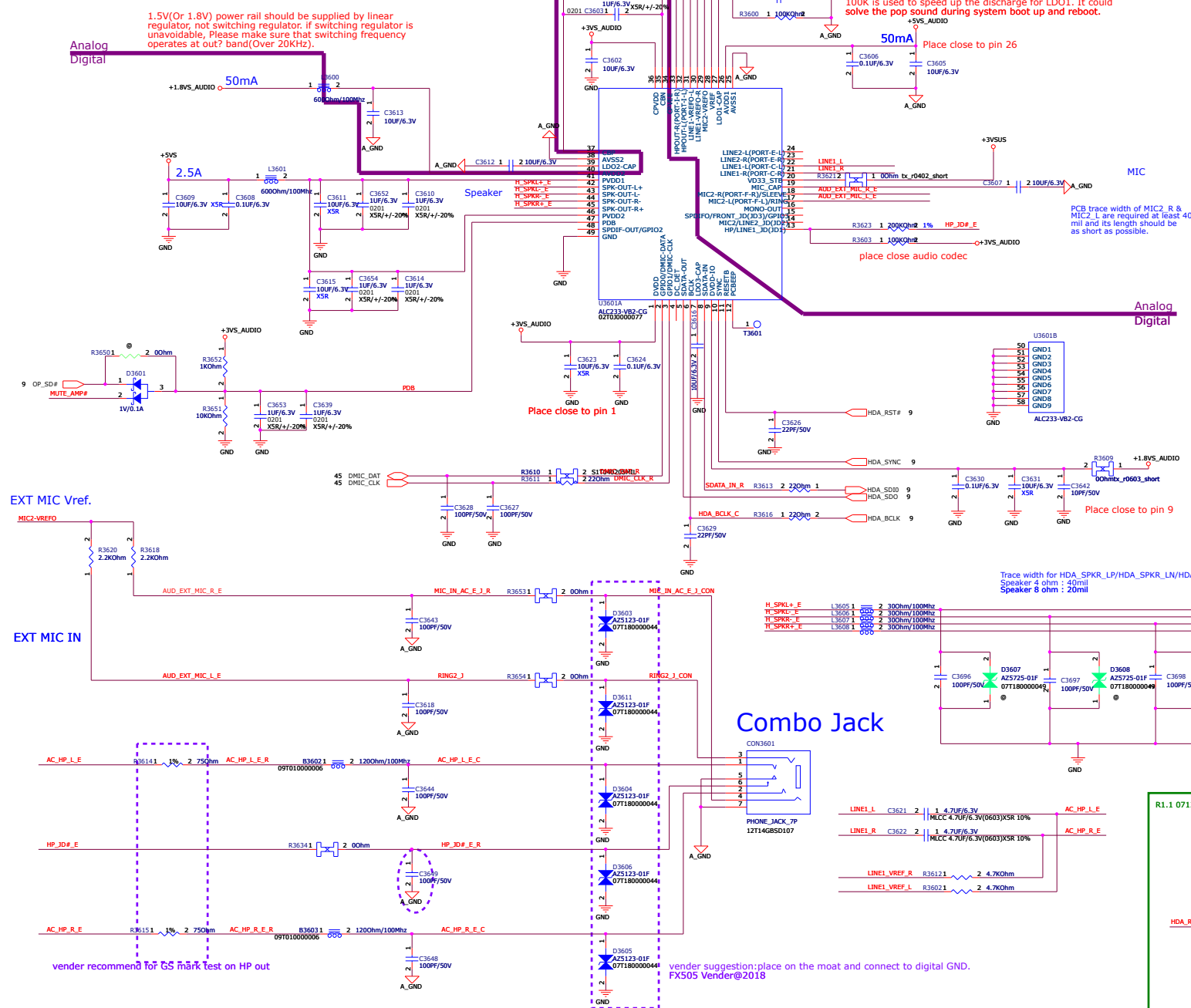


34. Transformer/RJ45

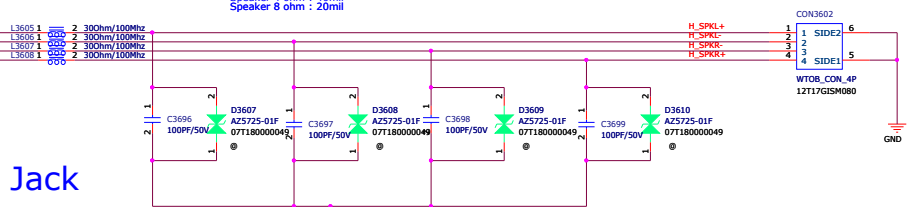




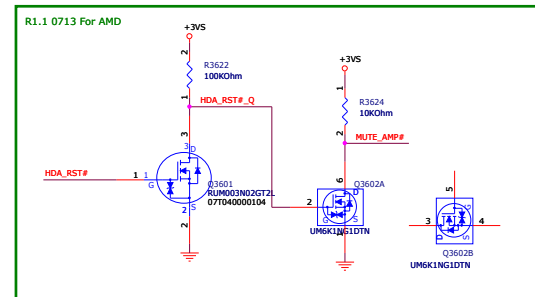
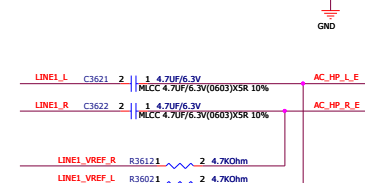
## ALC233-VB2-CG CODEC



## SPKR Conn.




## Combo Jack

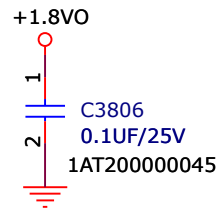
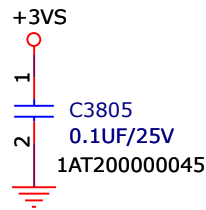
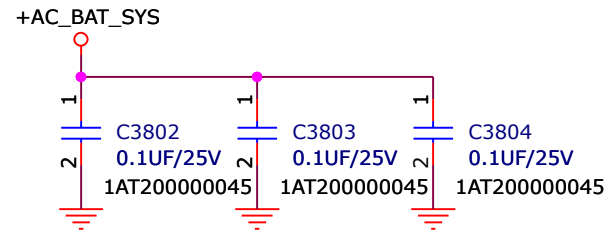
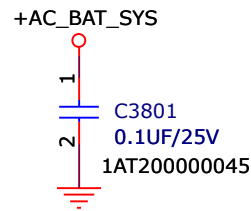
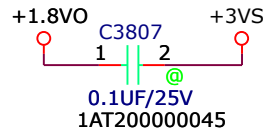




+AC\_BAT\_SYS

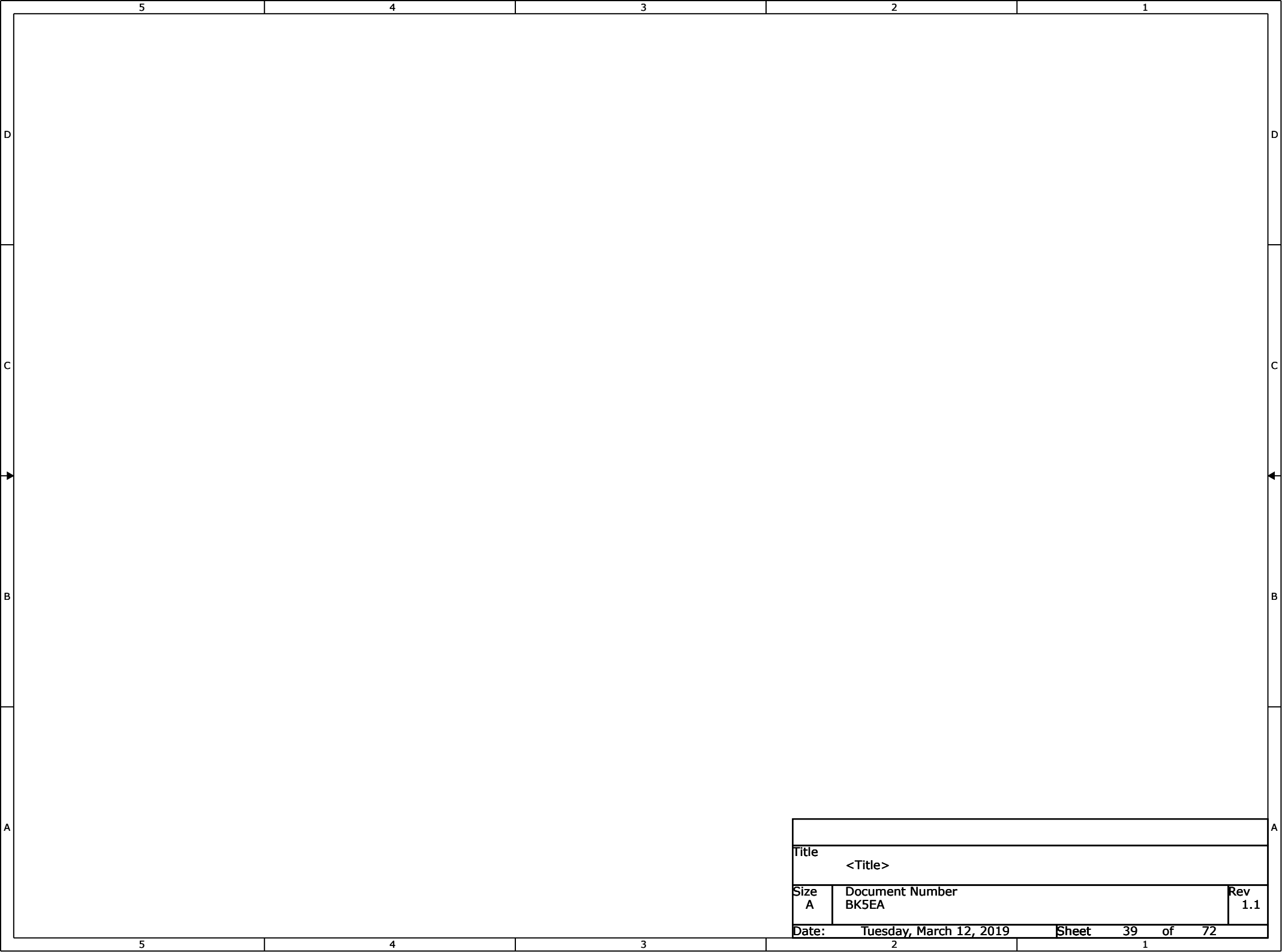


+AC\_BAT\_SYS 45,80,81,82,83,84,88,97



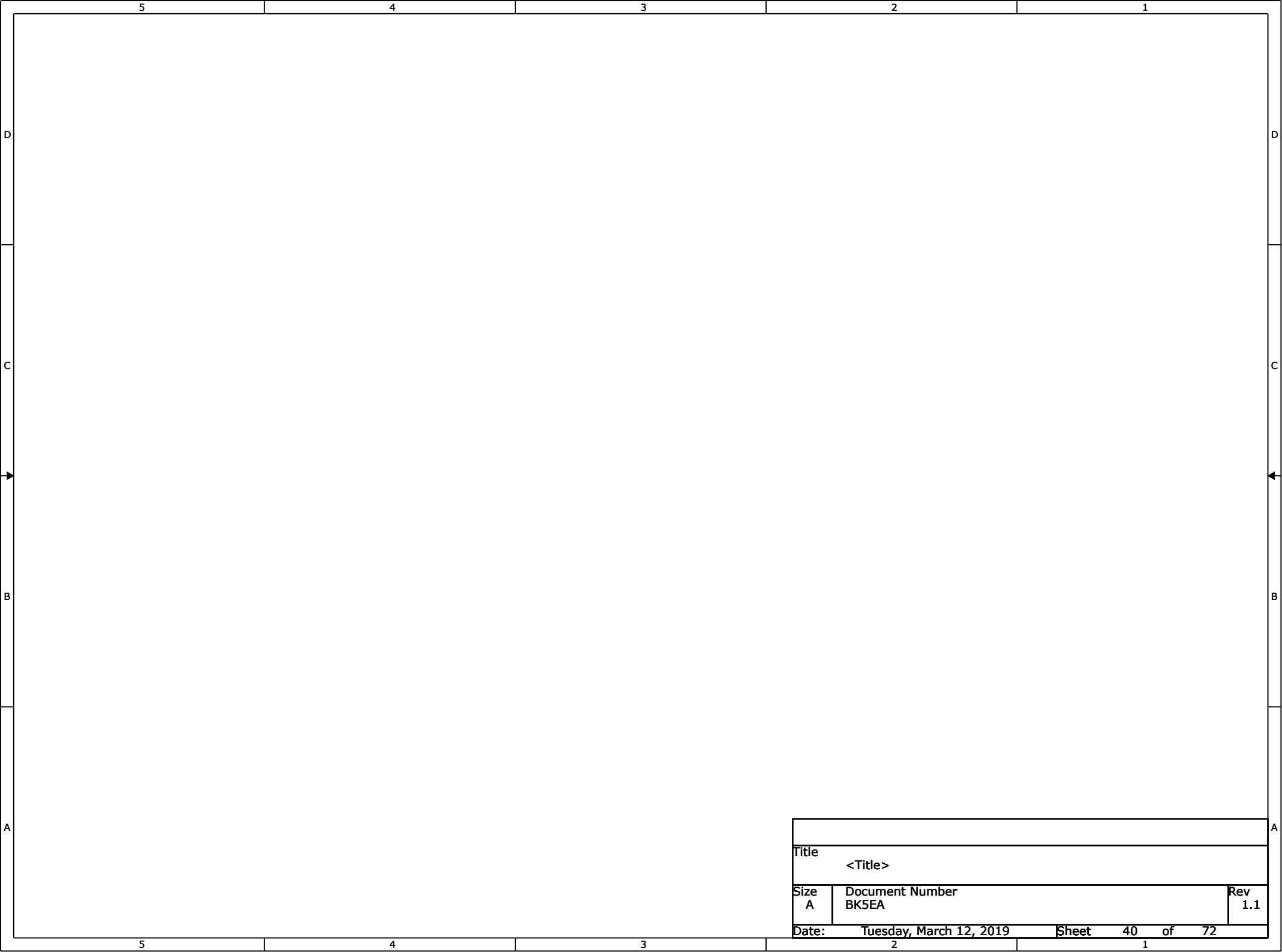
Title		
<Title>		
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Title			
<Title>			
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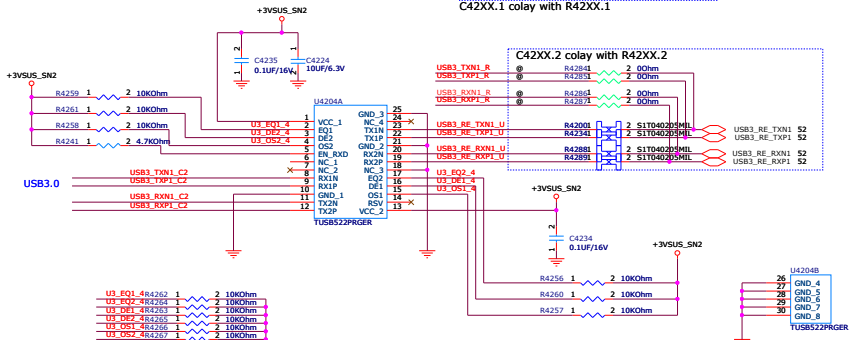




Title		
<Title>		
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### USB 3.0 PORT 1 (Gen 1)



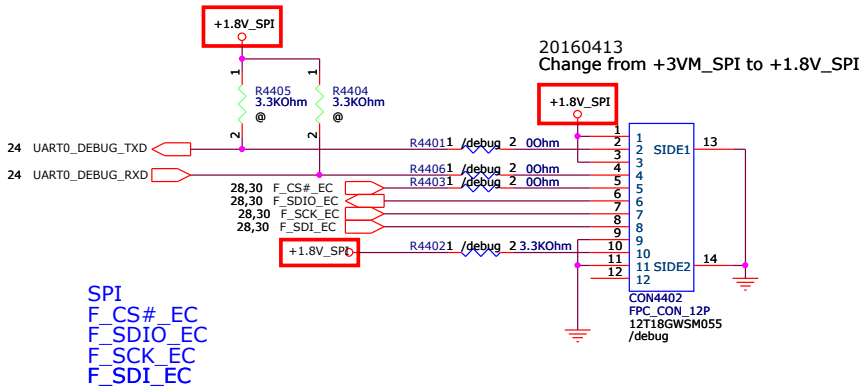
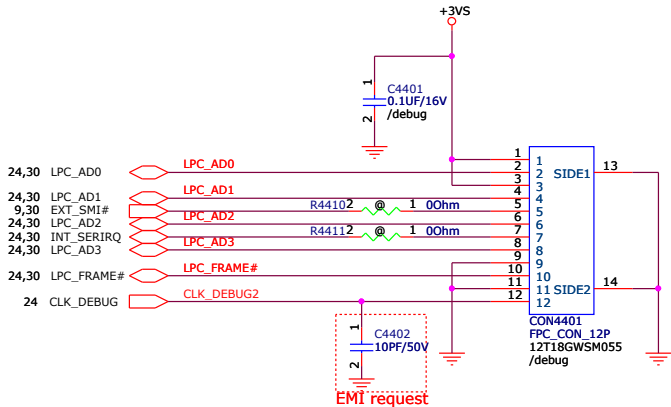
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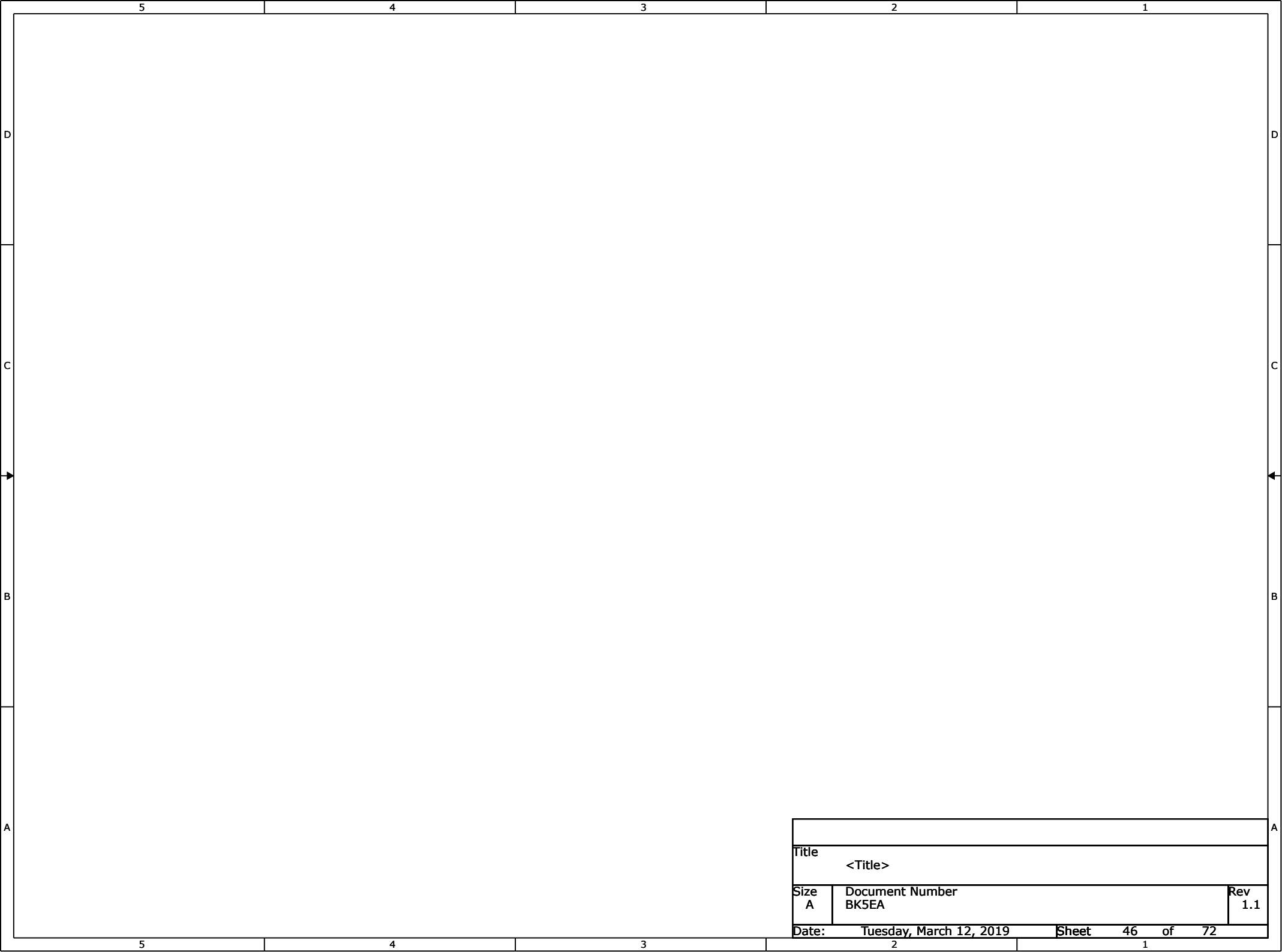
+3VS ○ +3VS 8,9,11,16,24,30,31,32,33,36,38,45,48,50,51,57,74,87,89,91,92,96  
 +3VSUS ○ +3VSUS 9,11,12,23,24,30,31,33,36,42,51,53,74,81,88,92,96  
 +3VM\_SPD ○ +3VM\_SPI





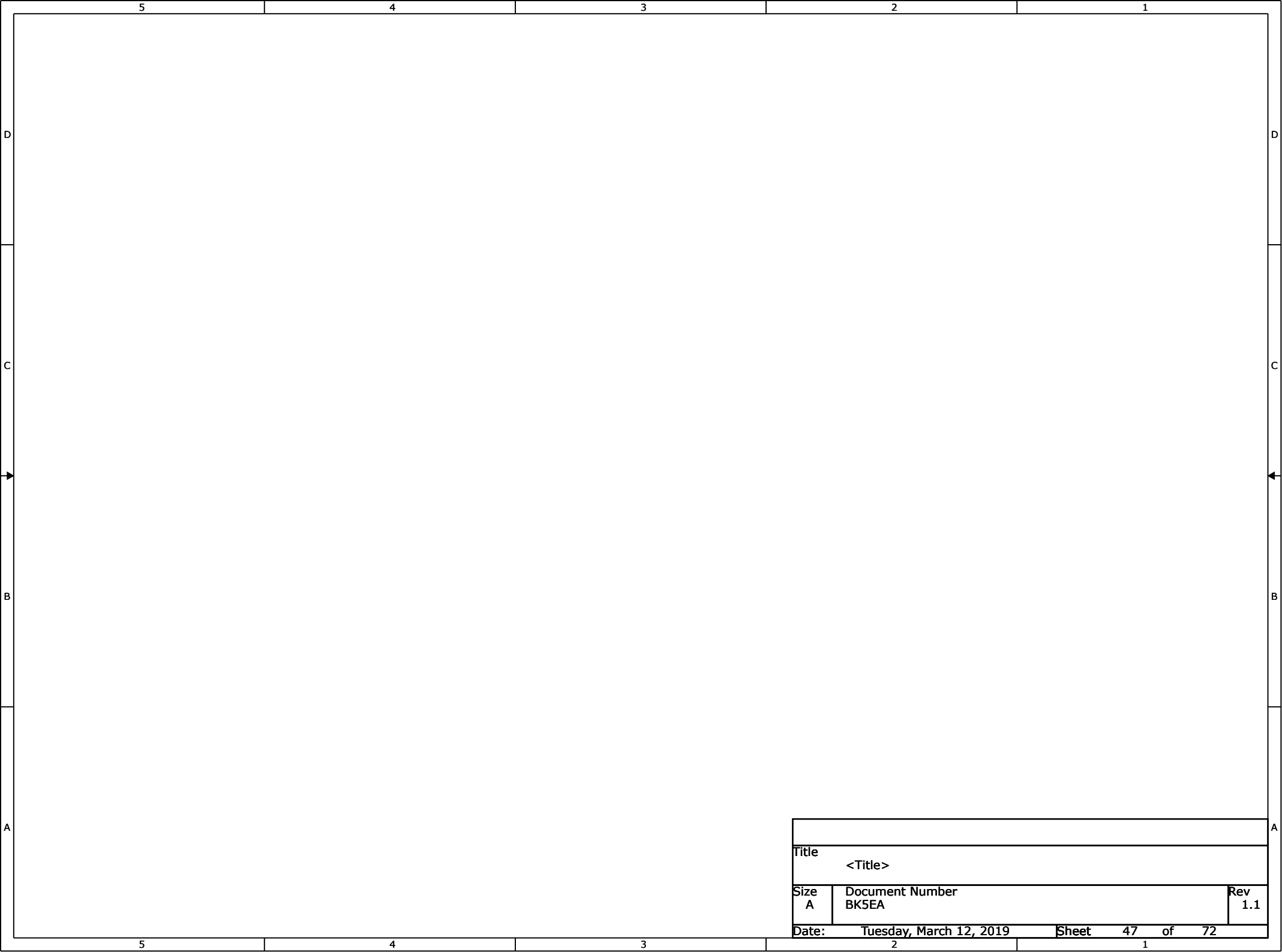






Title			
<Title>			
Size	Document Number		Rev
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2		1	

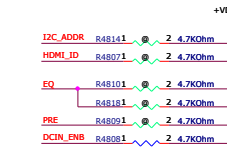
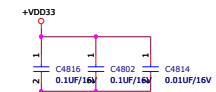
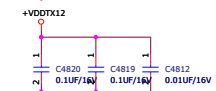
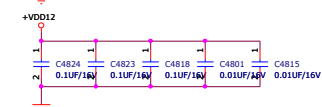
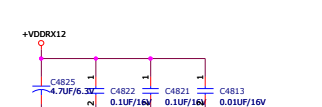
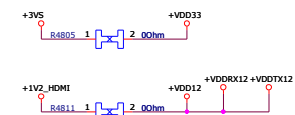
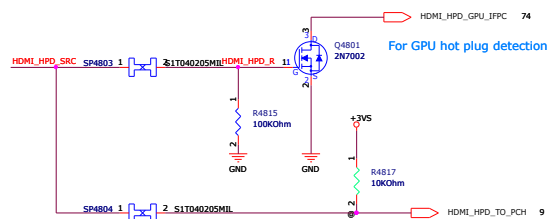
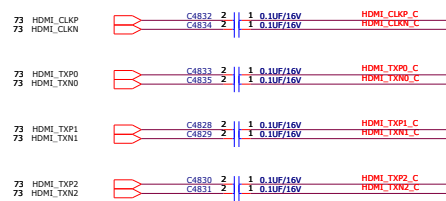




Title		
<Title>		
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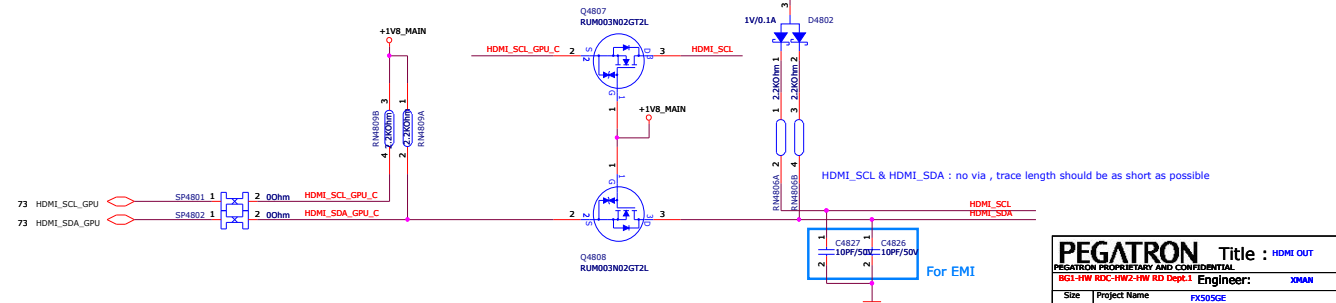
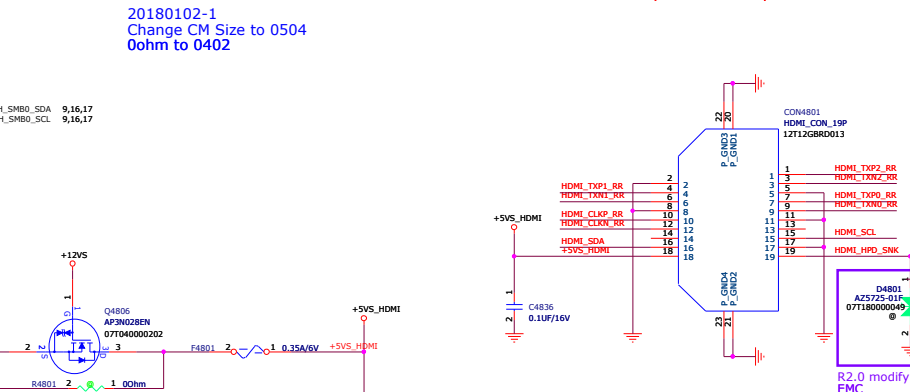
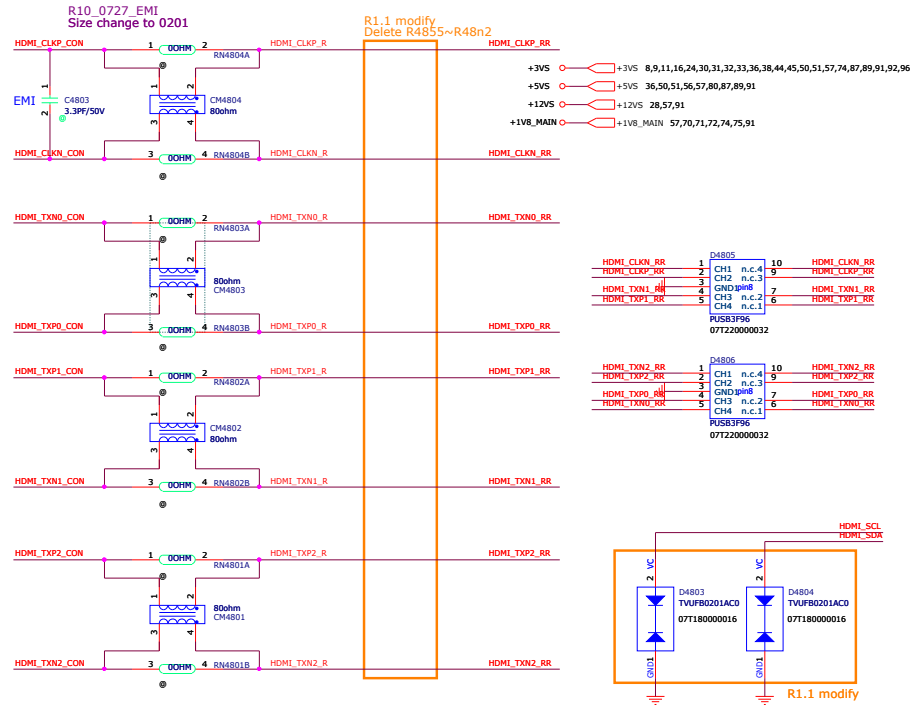
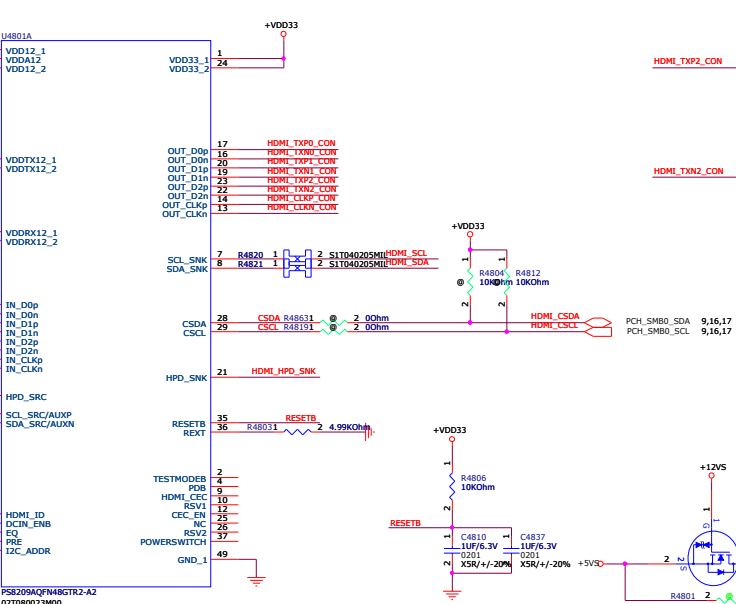
## HDMI



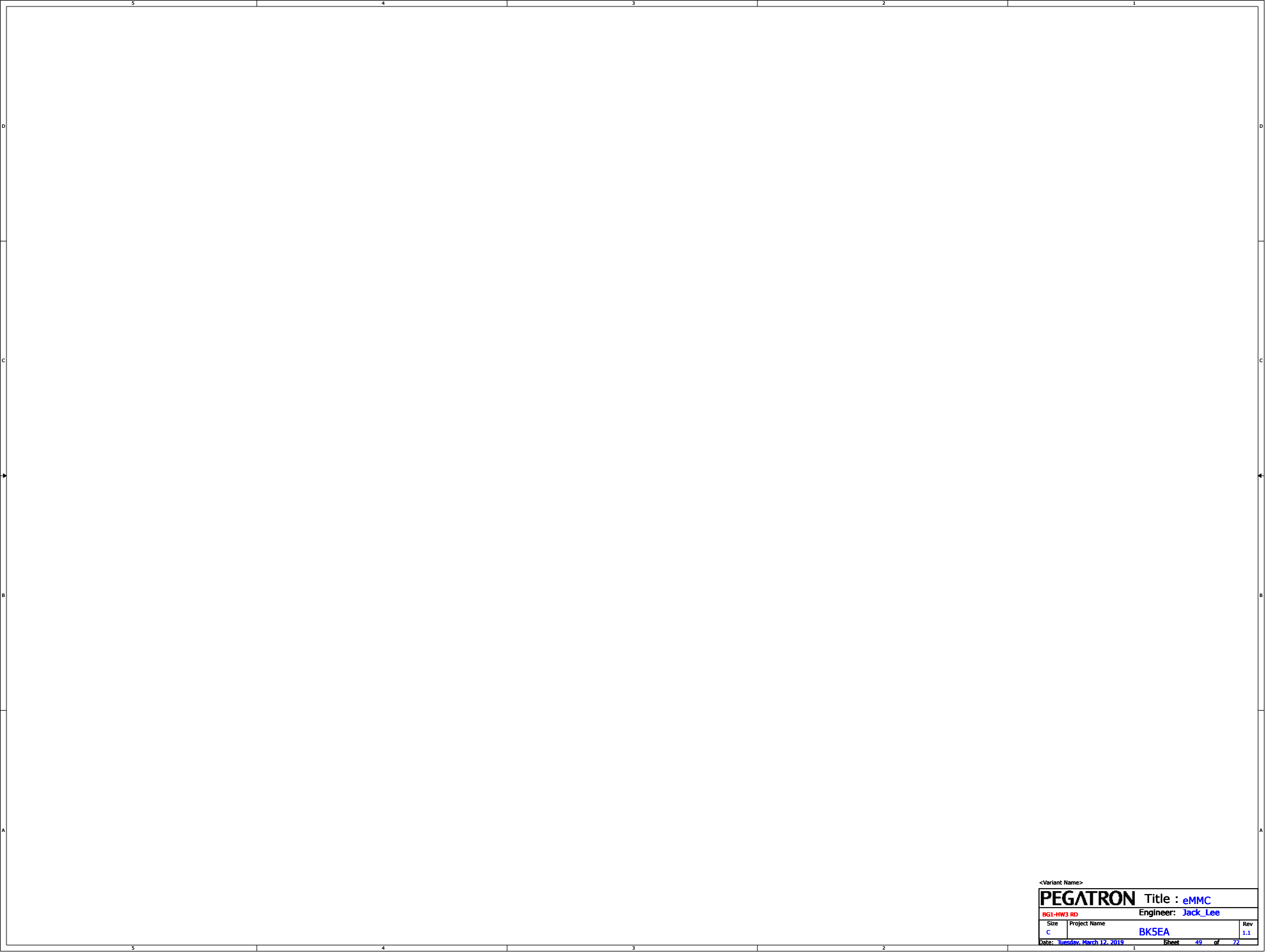
I2C slave address selection; Internal pull down  
L: Default, Slave address 0x10-2F  
H: Alternative slave address 0x90-9F; 0xD0-DF

HDMI ID enable; Internal pull down  
L: Default, HDMI ID enable  
**H: HDMI ID disable**

EQ -- Receiver equalization setting; Internal pull up  
L: Compensation for channel loss up to 13db  
H: Default, compensation for channel loss up to 17db  
M: Compensation for channel loss up to 11db  
  
PRE -- Output preemphasis setting; Internal pull up  
L: Pre-emphasis = 2.5db  
H: Default, No Pre-emphasis







<Variant Name>

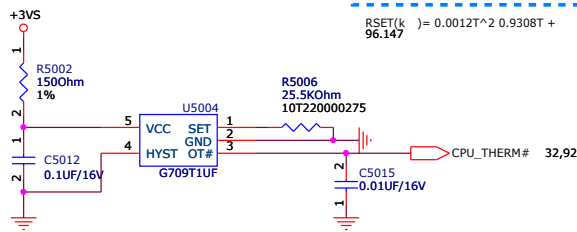
<b>PEGATRON</b>		Title : eMMC	
BG1-HW3 RD		Engineer: Jack_Lee	
Size	Project Name		Rev
C	BK5EA		1.1
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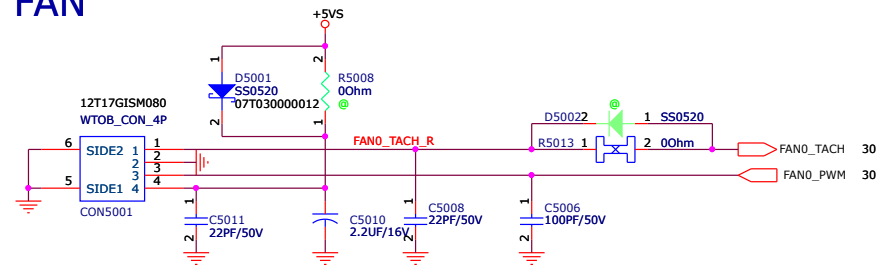
CPU Thermal Sensor

temperature set=85 C

$RSET(k) = 0.0012T^2 + 0.9308T + 96.147$

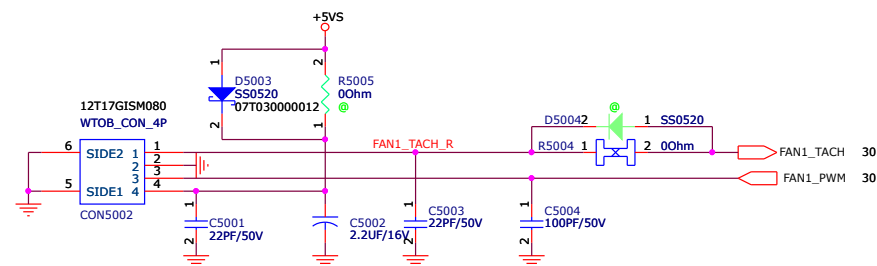


CPU FAN



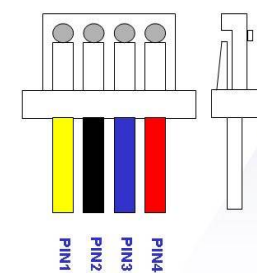
EC(PU@+3VS,10Kohm

GPU FAN



EC(PU@+3VS,10Kohm

4Pins Fan Connector Pins Definition

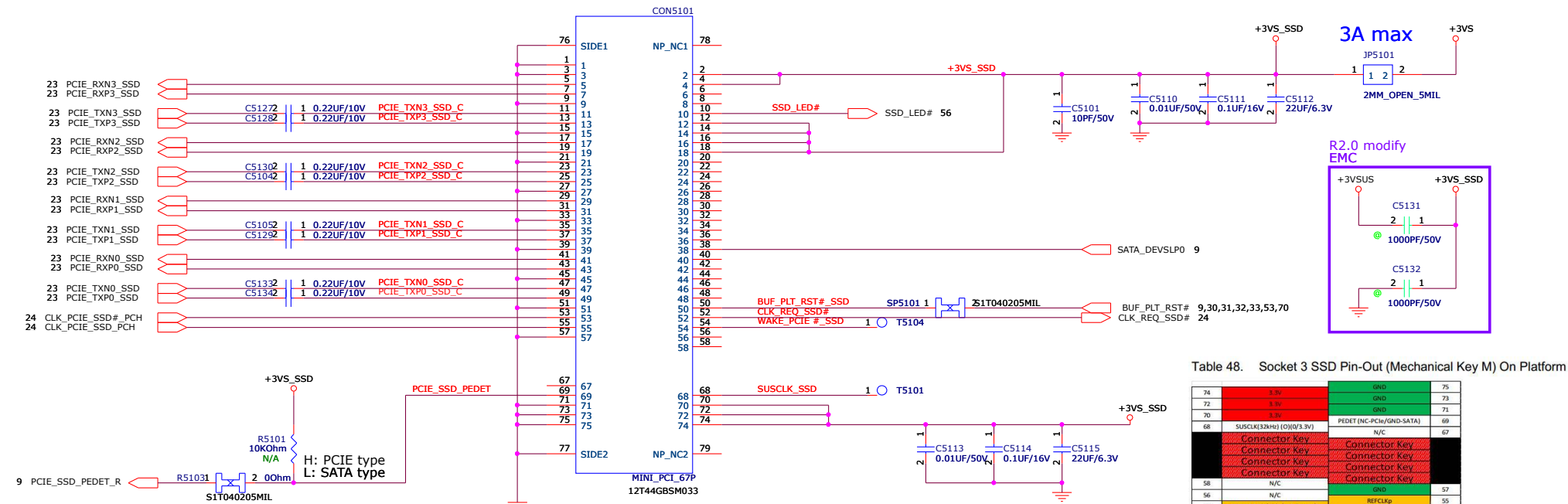


Pin No.	Function
Pin 1	TACHO
Pin 2	GNA
Pin 3	PWM
Pin 4	+5V

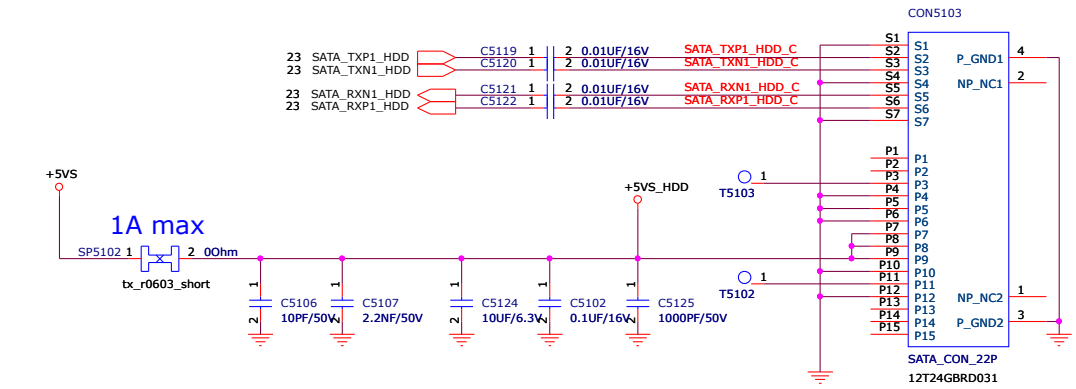


SSD/HDD

M.2 2280 KEY-M

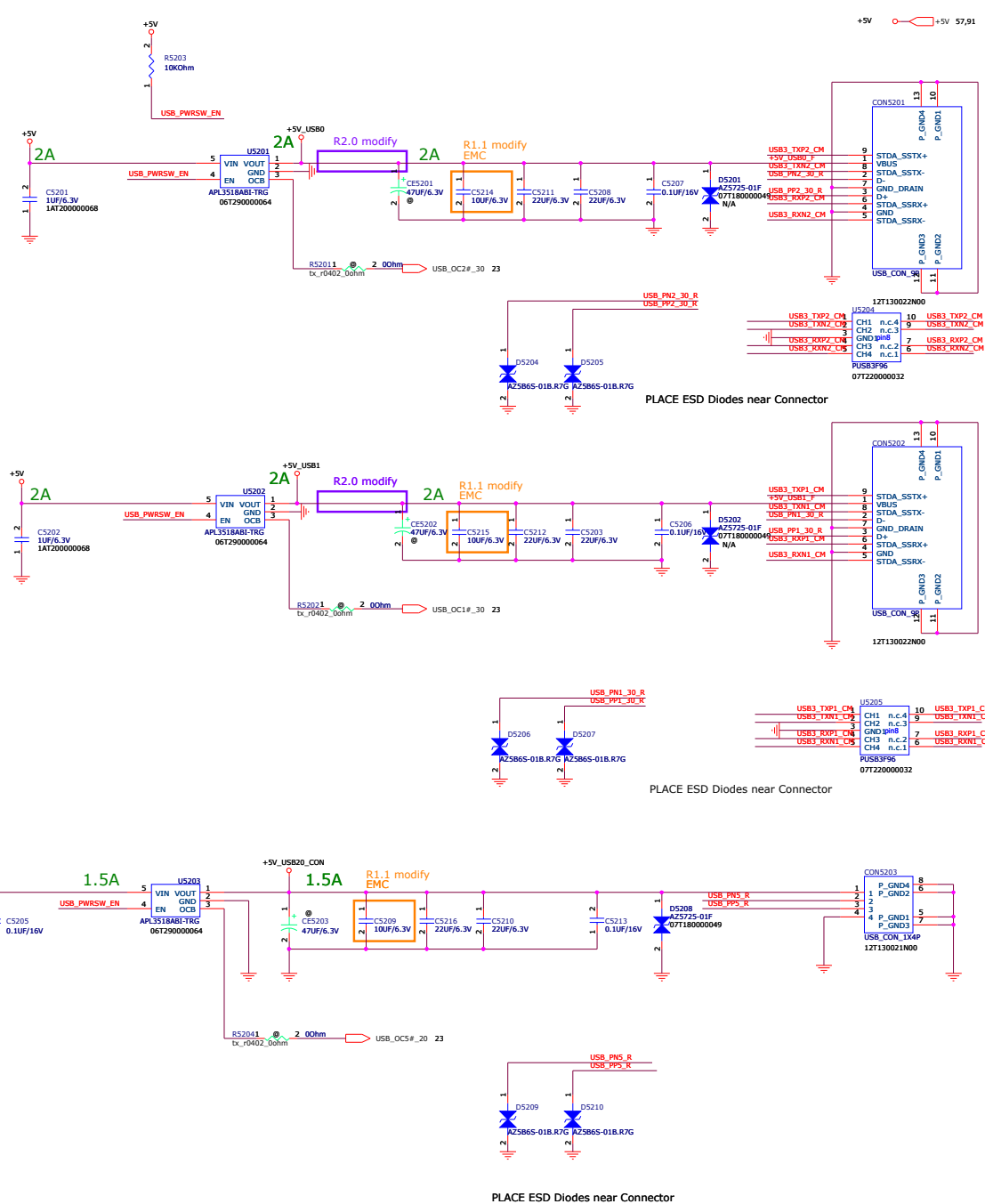
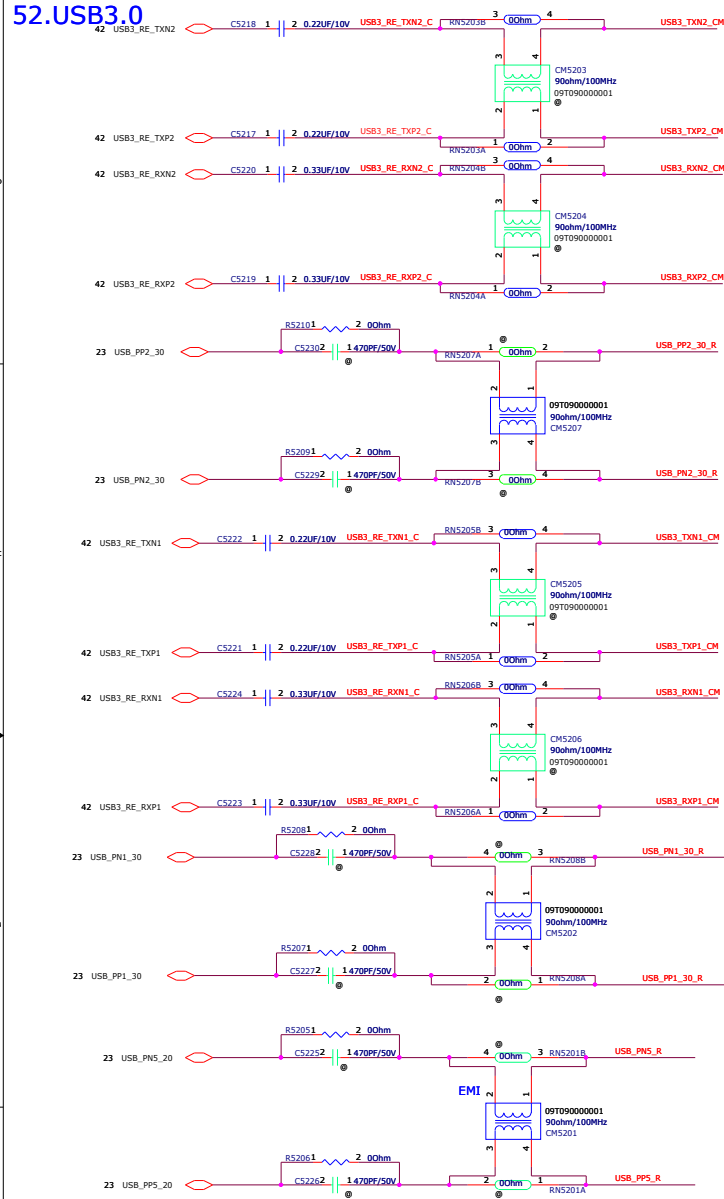


SATA Conn. 2.5"HDD





## 52.USB3.0

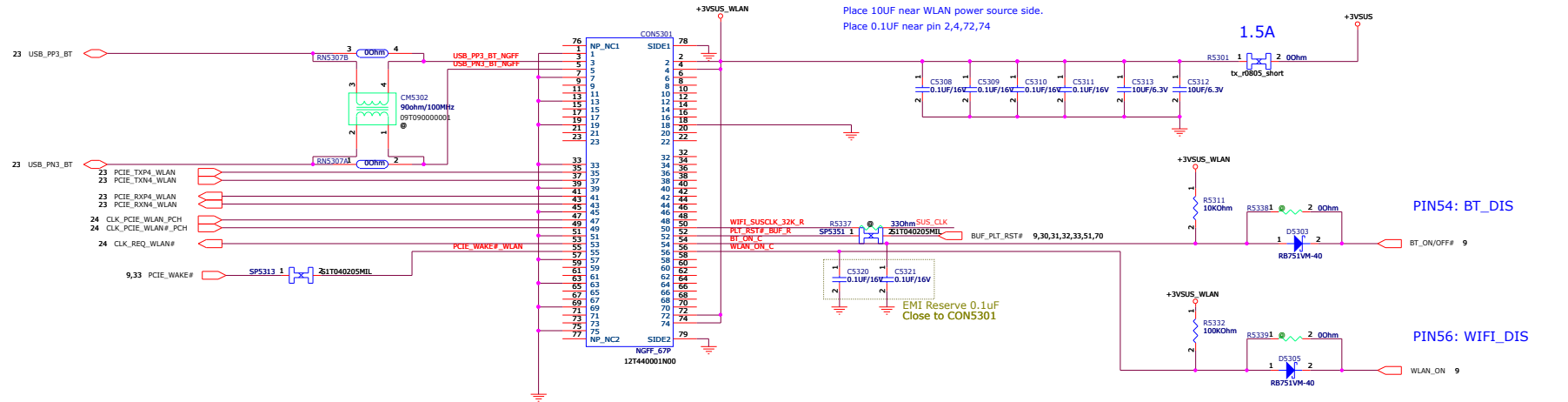




## WLAN+BT

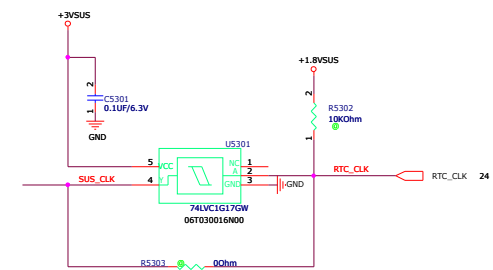
M.2 2230 KEY-E

WLAN bypass capacitors:

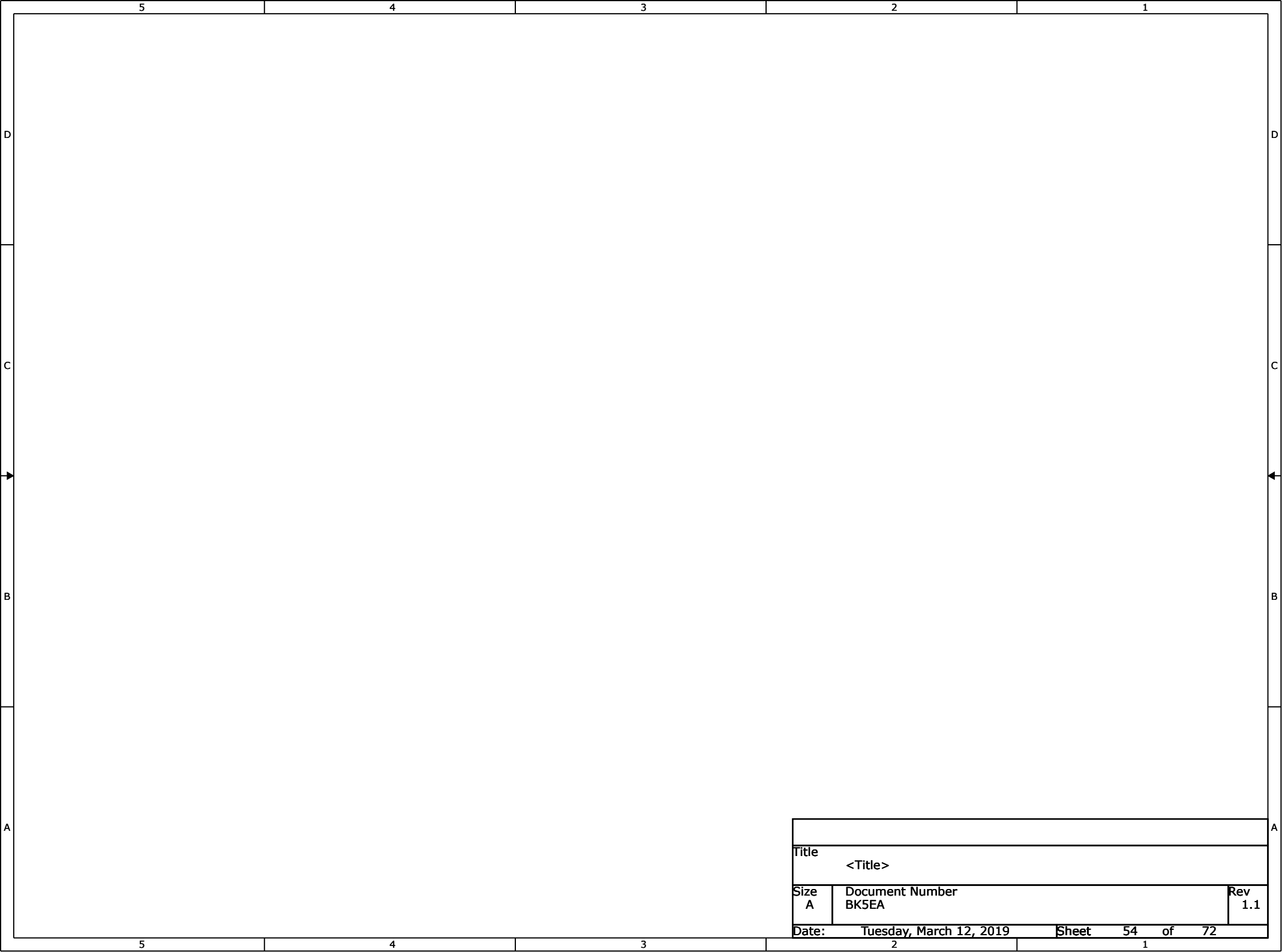


	Standard M.2 Key E	LoP Signals	LoP Signals	Standard M.2 Key E	
74	REFCLKP		GND	75	
72	REFCLKN		WT_CLKP	73	
70	PEWAKE#(IO[0]/Q3.3V)		WT_CLKN	71	
68	CLKREQD#(IO[0]/Q3.3V)		REFCLKP1	69	
66	PERST#(IO[0]/3.3V)		WT_D0N	67	
64	RESERVED	REFCLKIO1V(±95.4mHz)	WT_D0N	PETn1	
62	ALERT#(IO/L8)	AAMP_R0P	WT_D1P	PETp1	
60	I2C_CLK(IO[0]/1.8V)	AAMP_I2C_CLK	WT_D1P	PETn1	
58	I2C_DATA(IO[0]/1.8)	AAMP_I2C_DATA	WT_D1N	PETp1	
56	W_DISABLE#(IO[0]/Q3.3V)		GND	57	
54	W_DISABLE#(IO[0]/Q3.3V)		PEWAKE#(IO[0]/Q3.3V)	55	
52	PERST#(IO[0]/3.3V)		CLKREQD#(IO[0]/Q3.3V)	53	
50	SUSCLK(32kHz)(IO[0]/3.3V) ± 2.5% (3.3V Tolerant)		IOVDD	51	
48	COEX_TXD(IO[0]/1.8V)		REFCLK0	49	
46	COEX_RXD(IO[0]/1.8V)		REFCLKP0	47	
44	COEX_CK(IO[0]/1.8V)		REFCLKN	45	
42	CLINK_CLK		PERR0	43	
40	CLINK_DATA		PERP0	41	
38	CLINK_RESET(IO[0]/3.3V)		GND	39	
36	LPSS_UART_RTS(IO[0]/1.8V) / BRI_DT (MUX'd in PCH/SoC)		PETH0	37	
34	LPSS_UART_CTS(IO[0]/1.8V) / RGI_RST (MUX'd in PCH/SoC)		PTP0	35	
32	LPSS_UART_TX(OVDD/1.8V) / BRI_DT (MUX'd in PCH/SoC)		GND	33	
E	Connector Key		Connector Key		
	Connector Key		Connector Key		
	Connector Key		Connector Key		
	Connector Key		Connector Key		
	Connector Key		Connector Key		
22	LPSS_UART_R#(IO[0]/1.8V) / BRI_RST (MUX'd in PCH/SoC)		WGR_CLKP	SIO0_ResetM(IO[0]/1.8V)	23
20	UART_WAKE#(GND/IO/L8, LoP Production)		WGR_CLKN	SIO0_WAKE#(IO[0]/1.8V)	21
18	GND	LED0A_IOVDD_P0(LoP Production)	GND	SIO0_DATA#(IO[0]/1.8V)	19
16	LED0A_IOVDD		WGR_D0N	SIO0_DATA#(IO[0]/1.8V)	17
14	PCM_OUT(IO[0]/1.8V) / CLKREQ#(MUX'd in PCH/SoC)		WGR_D1N	SIO0_DATA#(IO[0]/1.8V)	15
12	PCM_IN(IO[0]/1.8V)		GND	SIO0_CMD#(IO[0]/1.8V)	13
10	PCM_SYNC(IO[0]/1.8V) / REF_RESET_B (MUX'd in PCH/SoC)		WGR_D1N	SIO0_CMD#(IO[0]/1.8V)	11
8	PCM_CLK(OVDD/1.8V)		GND	SIO0_CLK(IO[0]/1.8V)	9
6	LED0A_IOVDD		GND	GND	7
4	REFCLKP		REFCLKP	5	
2	REFCLKN		REFCLKN	3	
0	GND		GND	1	

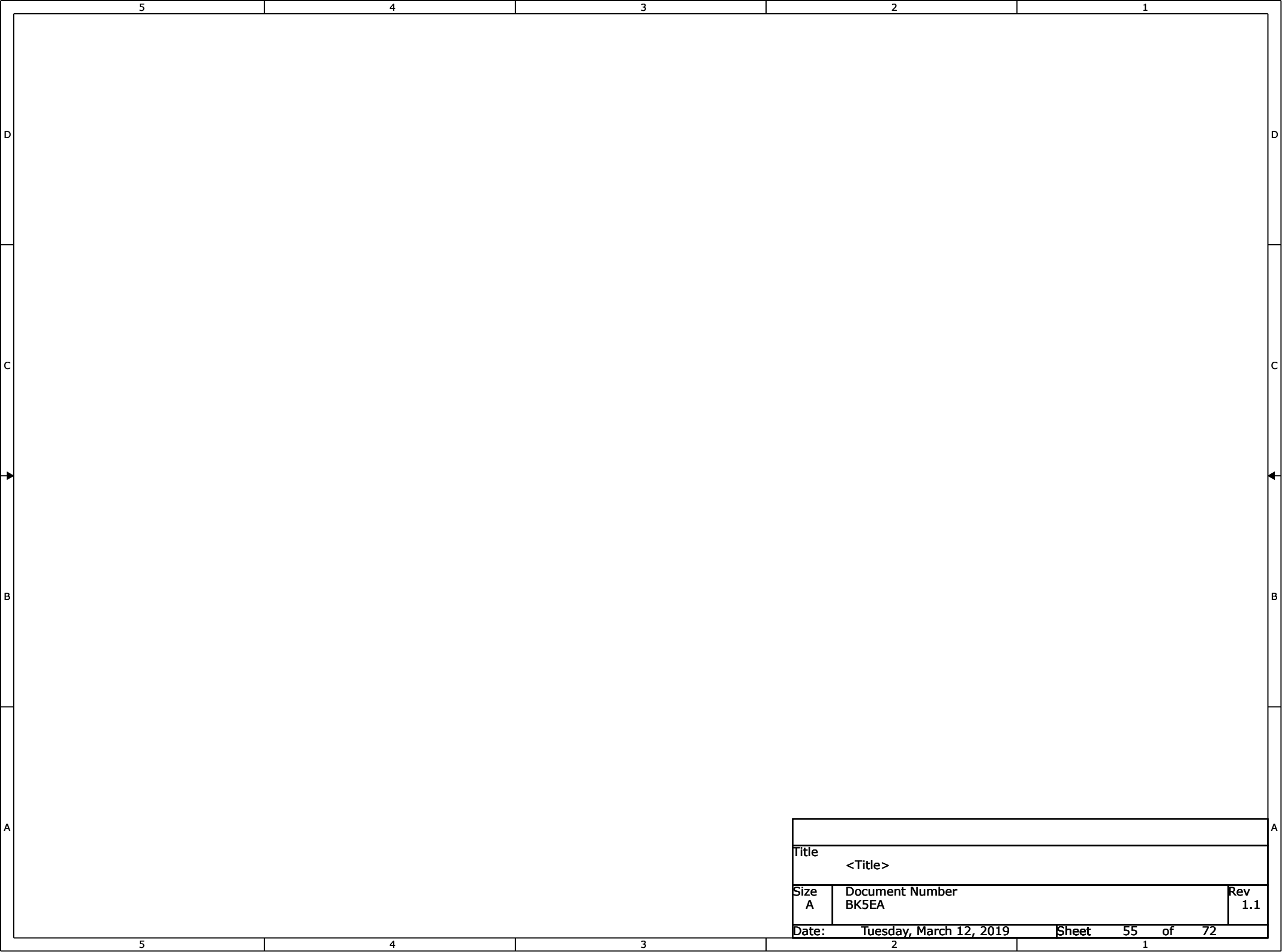
### WLAN\_SUS\_CLK Update





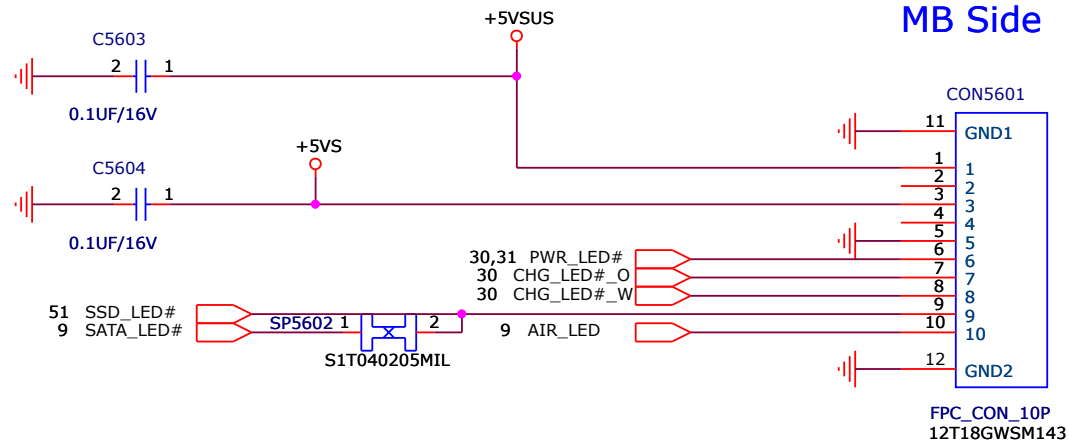






Title			
<Title>			
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+5VSUS 11,31,81

+5VS 36,48,50,51,57,80,87,89,91

Power LED

AIR PLANE LED

NOTE: AIR\_LED#\_R  
High -> airplane mode ON -> LED ON  
Low -> airplane mode OFF -> LED OFF

Charger LED

PCB/ID LOCATION

PWR LED  
LED5601

Charger LED  
LED5606

HDD LED  
LED5604

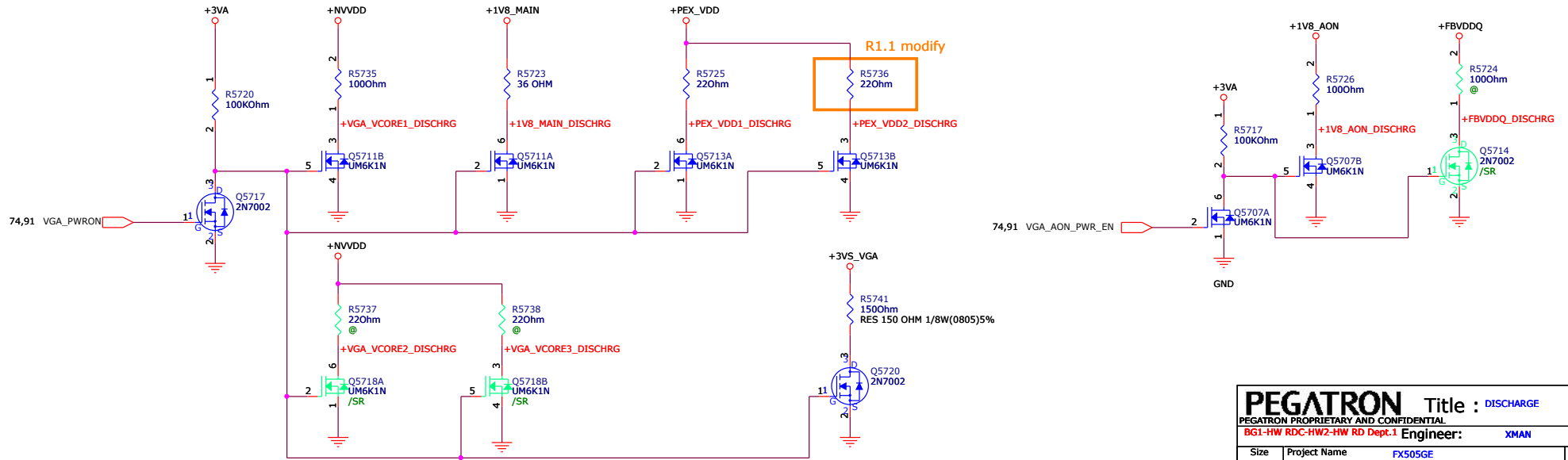
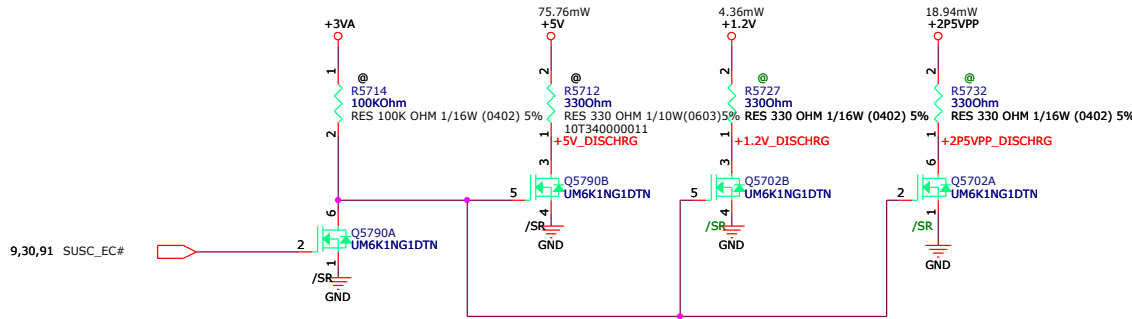
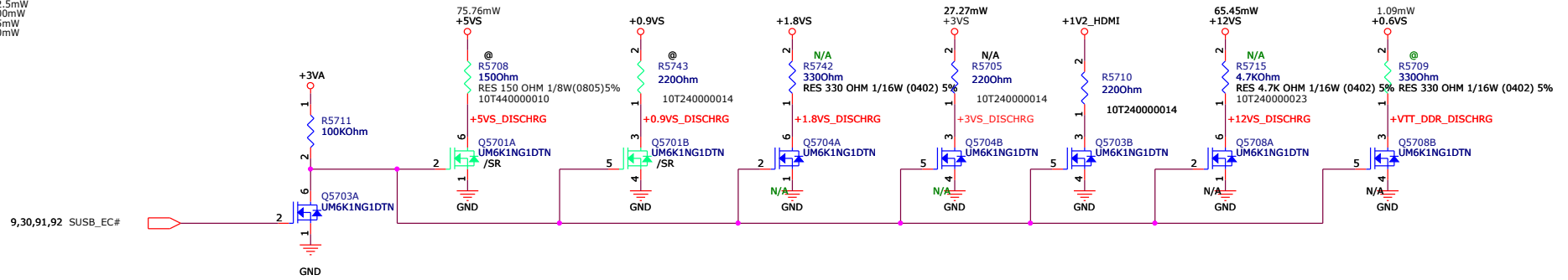
RF LED  
LED5602

HDD LED

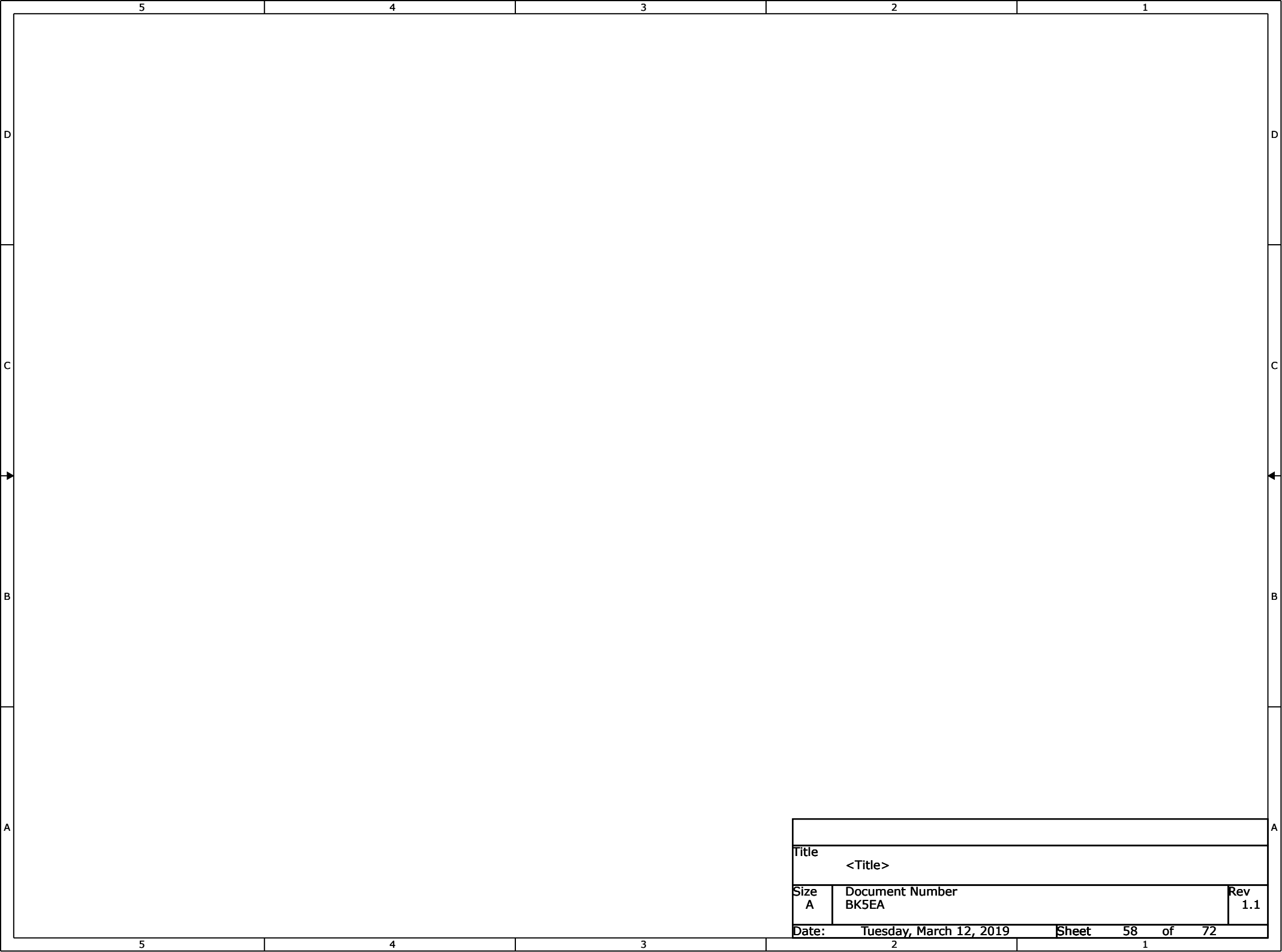
<b>PEGATRON</b>		Title : LED	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RDC-HW2-HW RD Dept.		Engineer: XMAN	
Size A4	Project Name Tuesday, March 12, 2019	Rev 56 72	Rev 1.0
Date:		Sheet of	



$V^2/R$   
 0402 = 1/16W = 62.5mW  
 0603 = 1/10W = 100mW  
 0805 = 1/8W = 125mW  
 1206 = 1/4W = 250mW

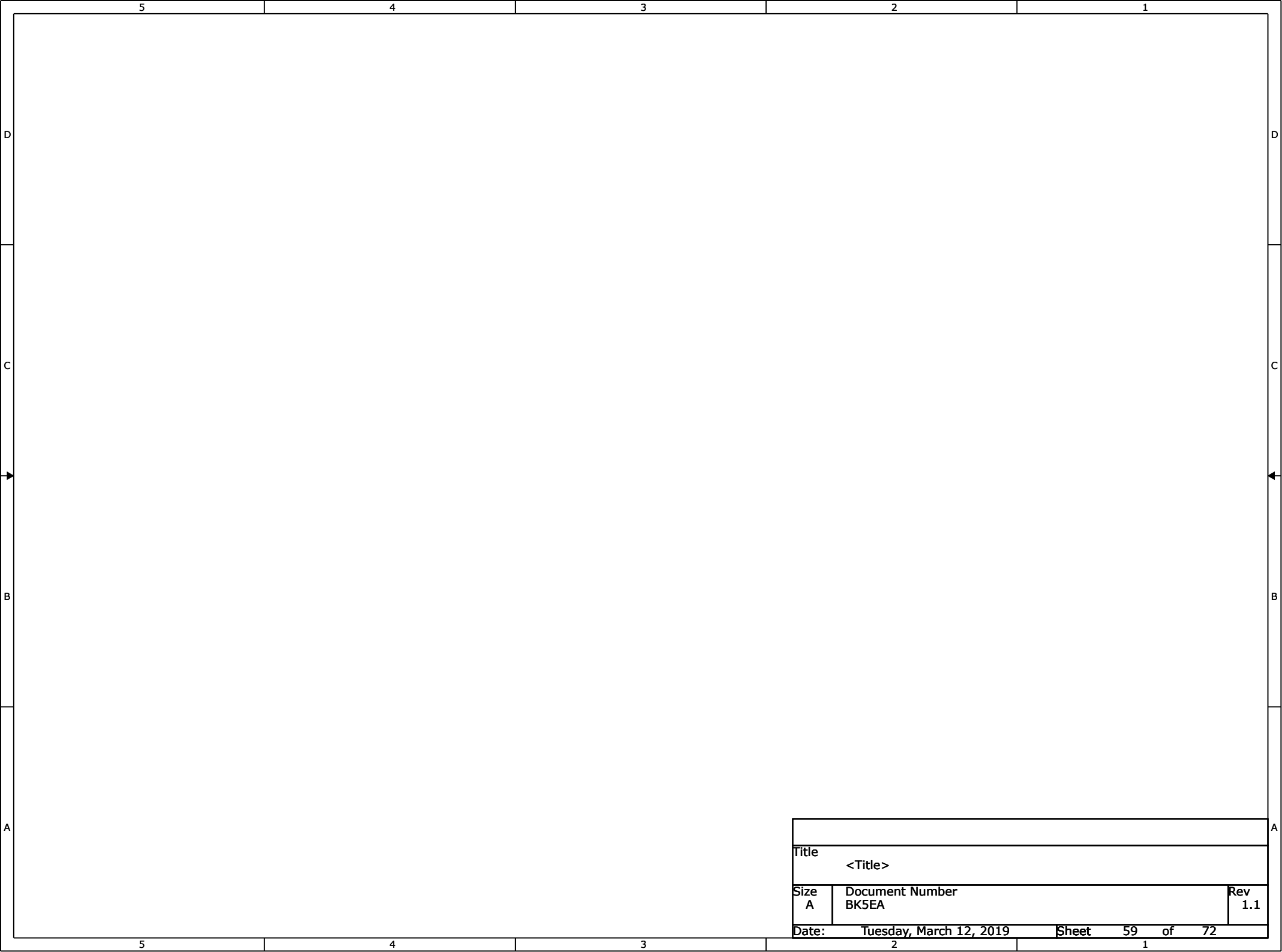






Title			
<Title>			
Size	Document Number		Rev
A	BK5EA		1.1
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2		1	

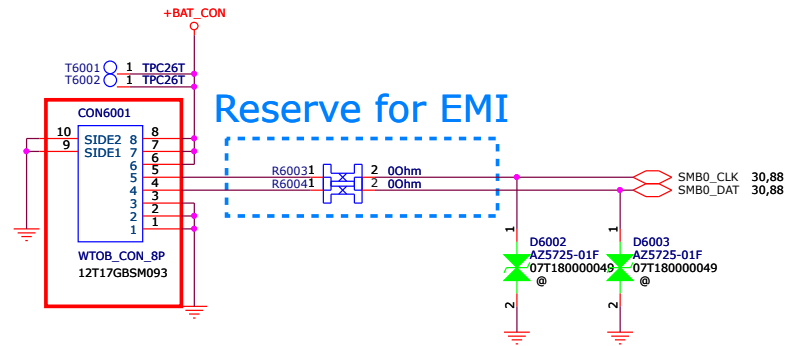




Title			
<Title>			
Size	Document Number		Rev
A	BK5EA		1.1
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2		1	

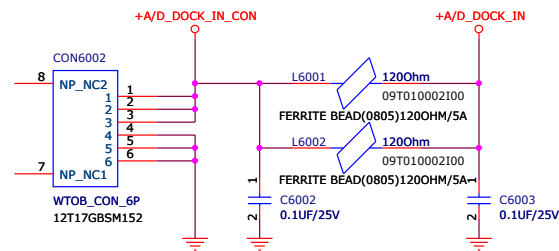


### Battery Conn.



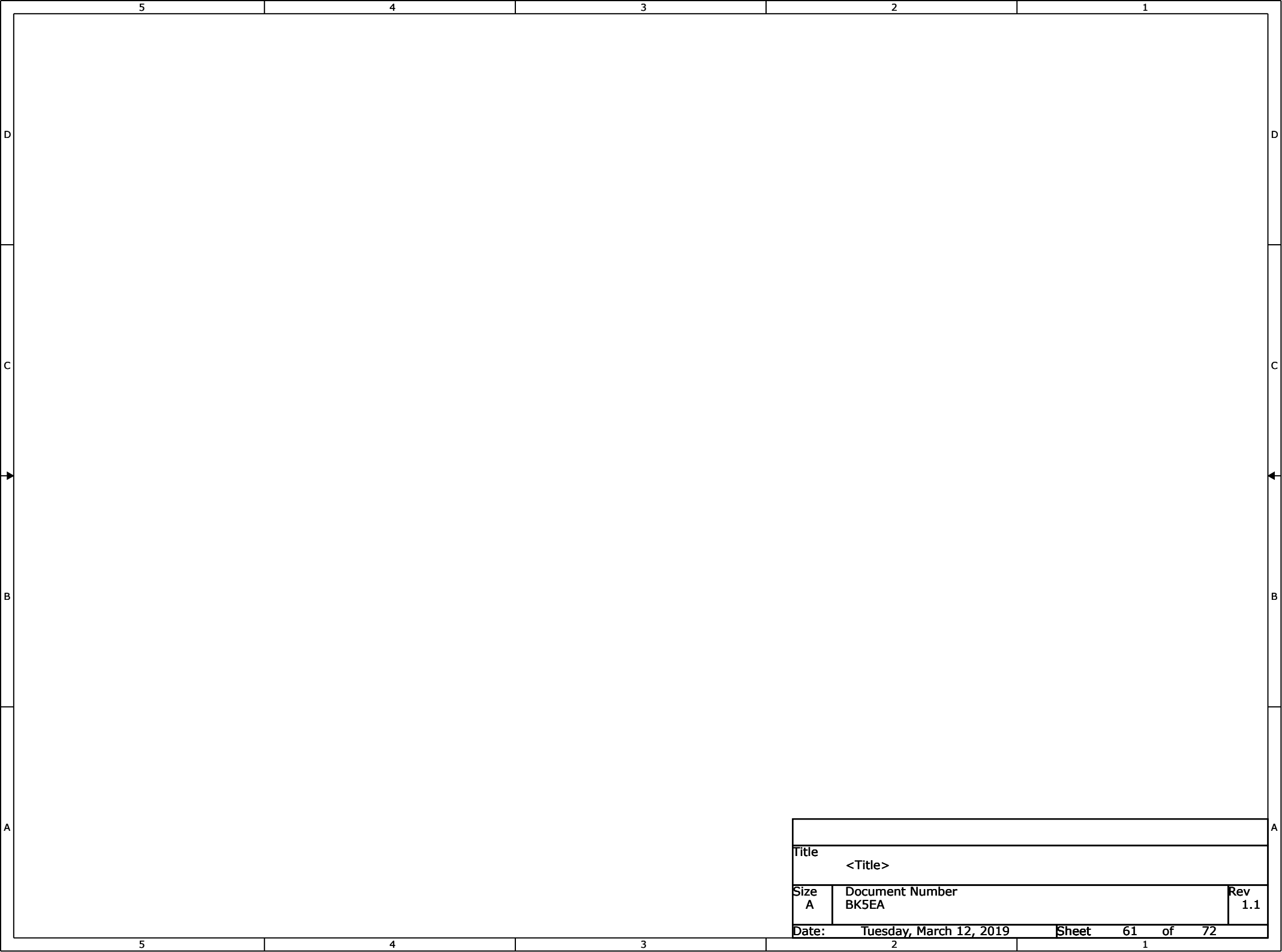
ABBA assign: 1217-01UG0AS(1217-017L000) doesn't include 1217-01EG000 (the same pool)

### AC in Conn.



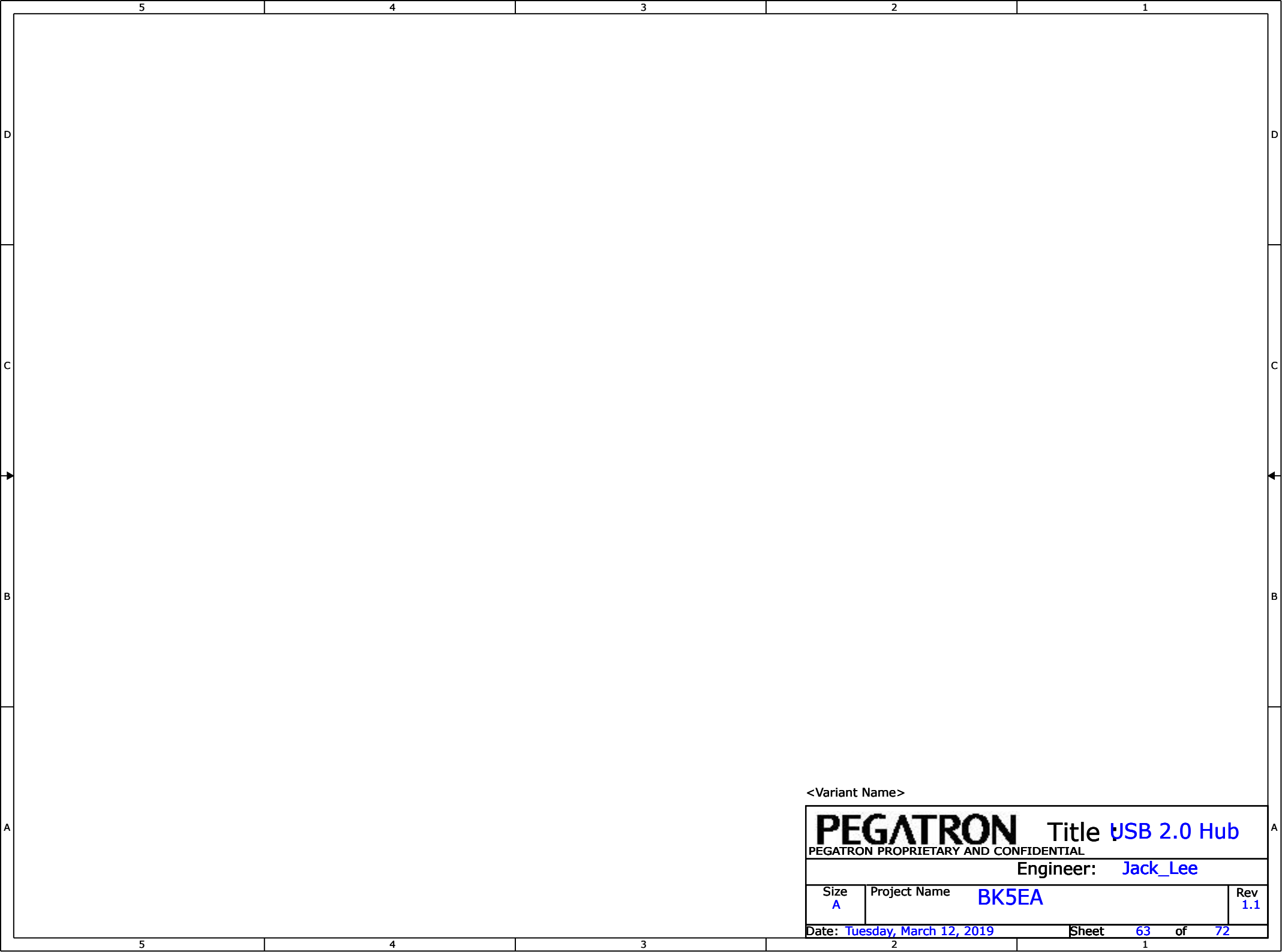
FX505GE N17P Adaptor: 120W  
FX505GM N17E Adaptor: 150W





Title			
<Title>			
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<Variant Name>

PEGATRON

Title USB 2.0 Hub

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Jack\_Lee

Size A	Project Name BK5EA	Rev 1.1
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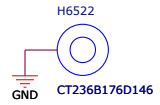
Date: Tuesday, March 12, 2019

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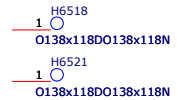
n5.NUT,Screw hole,Tooling hole

M.2 SSD NUT:



Tooling hole

drill 3\*3.5



drill 1.7

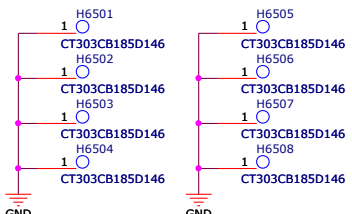


drill 2.2\*1.7

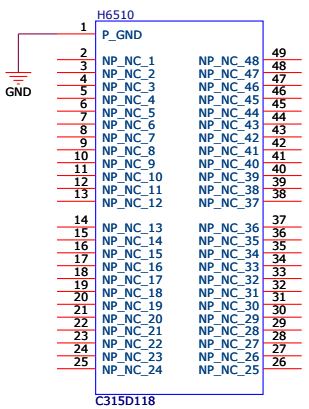


Screw hole

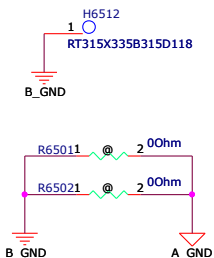
B group:  
CPU GPU bracket hole



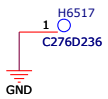
D group:



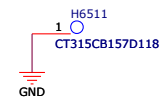
Near Audio Jack  
TOP: square 8  
BOT: phi 8 drill 3



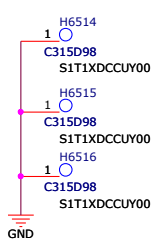
E:  
TOP: phi 7 drill 6  
BOT: phi 7 drill 6



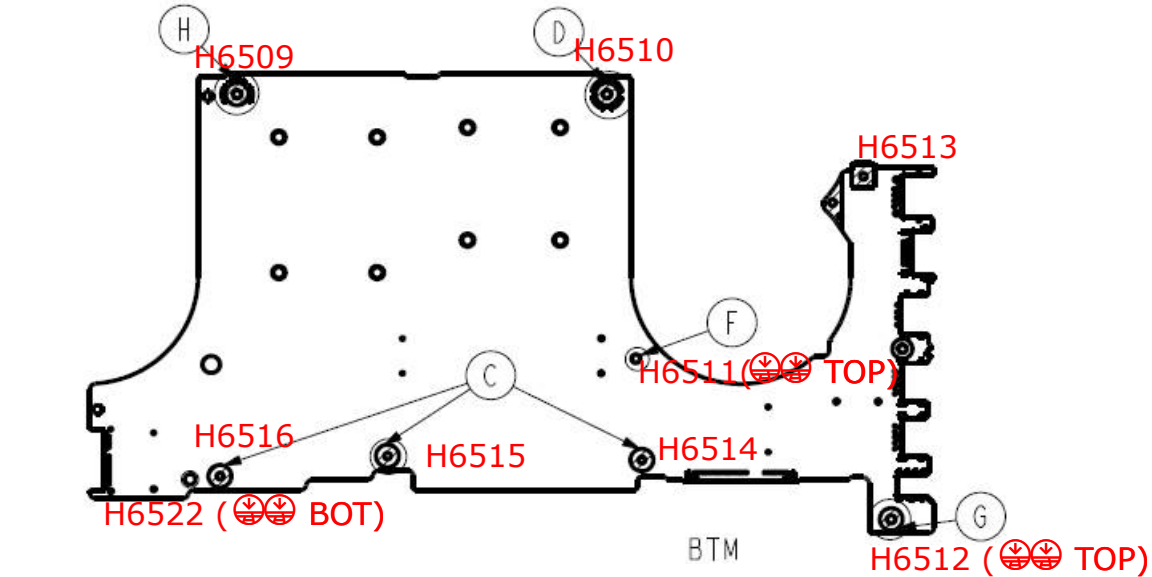
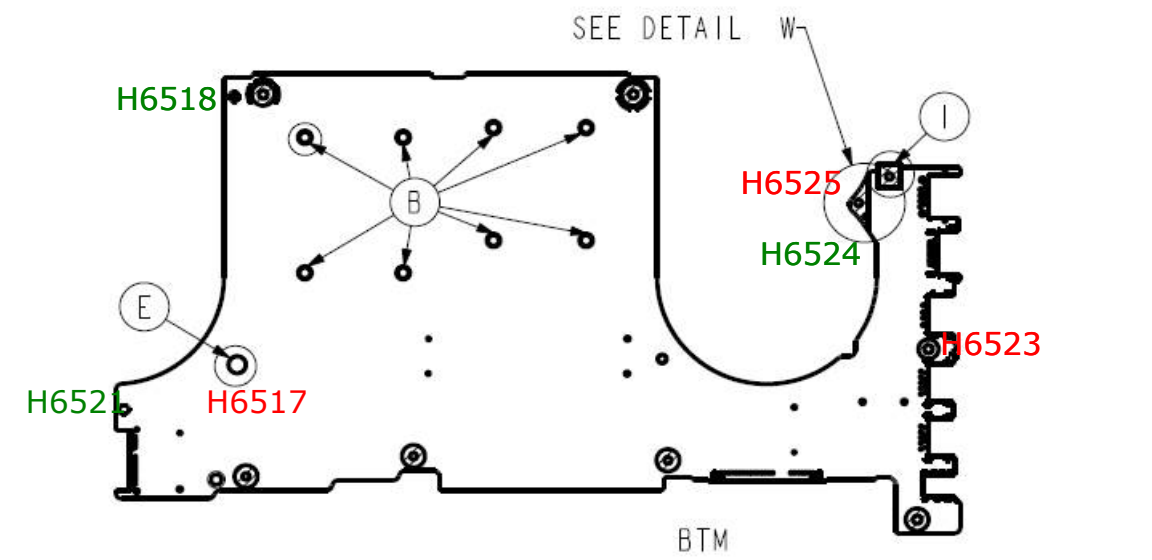
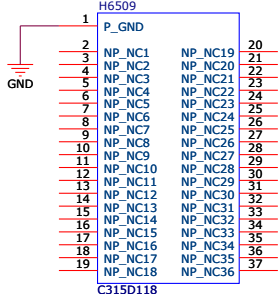
F:  
TOP: phi 8 drill 3  
BOT: phi 4 drill 3



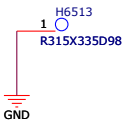
C group:  
TOP: phi 8 drill 2.5  
BOT: phi 8 drill 2.5



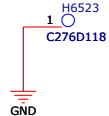
H group:



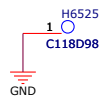
I group:  
TOP: square8\*8.5 drill 2.5  
BOT: square8\*8.5 drill 2.5



TOP: phi 7 drill 3  
BOT: phi 7 drill 3

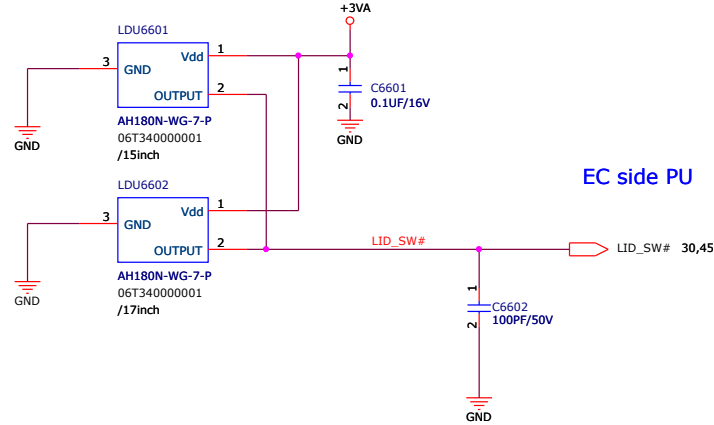


TOP: phi 3 drill 2.5  
BOT: phi 3 drill 2.5

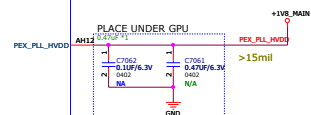
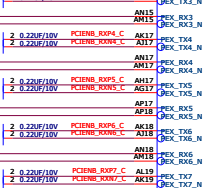
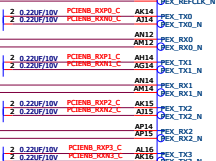
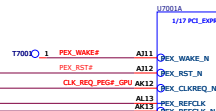




# Hall sensor







GPU	Capacity/Type	Footprint	Population #16 #17	Utilization
<b>PCI_VRD0 Supply Rate</b>				
GB4C-128, GB4D-128	1.0 μ <sup>3</sup>	565	0/0	0 Under GPU
	0.47 μ <sup>3</sup>	565	32/0	0 Under GPU
	4.7 μ <sup>3</sup>	565	0/2	2 Near GPU
	4.7 μ <sup>3</sup>	565	3/0	0 Under GPU
	10 μ <sup>3</sup>	55R	0/0	1 Midway between GPU and power supply
	10 μ <sup>3</sup>	55R	0/0	3 Near GPU
	22 μ <sup>3</sup>	55R	0/0	1 Midway between GPU and power supply
	22 μ <sup>3</sup>	565	0/0	0 Near GPU
<b>PCI_VRD0 Supply Rate</b>				
GB4C-128, GB4D-128	1.0 μ <sup>3</sup>	565	0/0	0 Under GPU
	0.47 μ <sup>3</sup>	565	0/0	0 Under GPU
	4.7 μ <sup>3</sup>	565	0/0	0 Under GPU
	4.7 μ <sup>3</sup>	565	0/3	0 Under GPU
	10 μ <sup>3</sup>	55R	0/0	2 Midway between GPU and power supply
	10 μ <sup>3</sup>	55R	0/0	3 Near GPU
	22 μ <sup>3</sup>	55R	0/0	1 Midway between GPU and power supply
	22 μ <sup>3</sup>	565	0/0	0 Near GPU

				Population		
GPU	Capacitor Type		Footprint	N18	N17	Location
PEX_PLL_HVDD Supply Rail						
GB4C-128,	0.1 $\mu$ F	X7R	0402	0	1	Under GPU
GB4D-128	0.47 $\mu$ F	X6S	0201W	1	0	Under GPU

Note:

- Decoupling for PEX\_PLL\_HVDD is merged with PEX\_HVDD, and Design may alternatively use two 0201W 0.47  $\mu$ F X6S for each 0201W 1  $\mu$ F.

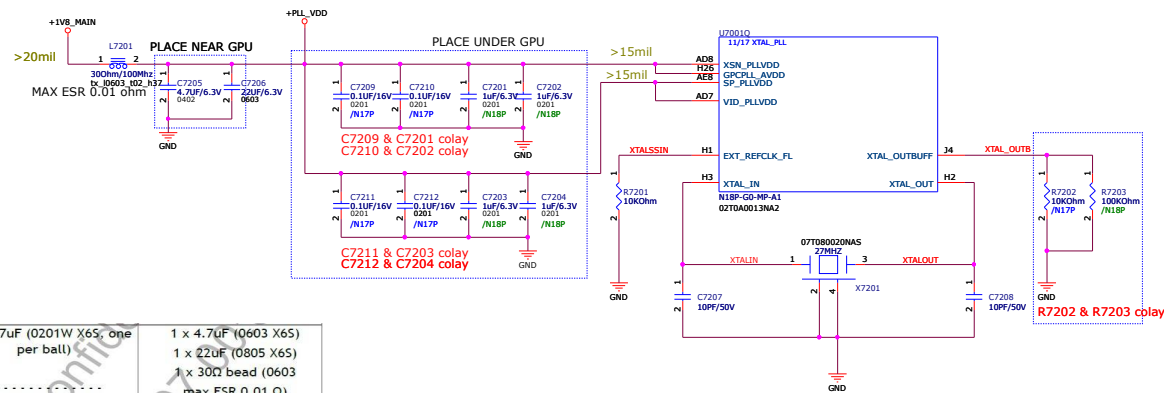
Rail (GPU Ball)	Balls	Voltage	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	14 x 0.47uF (0201W X65) 3 x 4.7uF (0603 X65)  Alternate solution: 7 x 1uF (0402 or 0201W, X65) <sup>1</sup> 3 x 4.7uF (0603 X65)	3 x 10uF (0805 X65) 2 x 22uF (0805 X65)
PEX_DVDD	6	1.0V	12 x 0.47uF (0201W X65) 3 x 4.7uF (0603 X65)  Alternate solution: 6 x 1uF (0402 or 0201W, X65) <sup>1</sup> 3 x 4.7uF (0603 X65)	3 x 10uF (0805 X65) 2 x 22uF (0805 X65)



NVIDIA (N17P)  
DA-07679-001\_v05 P.37  
-----  
XS\_PLLVDD  
Under GPU (Put at GPCPLL\_AVDD side)  
No capacitors

NVIDIA (N17P)  
DA-07679-001\_v05 P.38  
-----  
SP\_PLLVDD/VID\_PLLVDD  
Under GPU  
0.1uF x2 (0402)

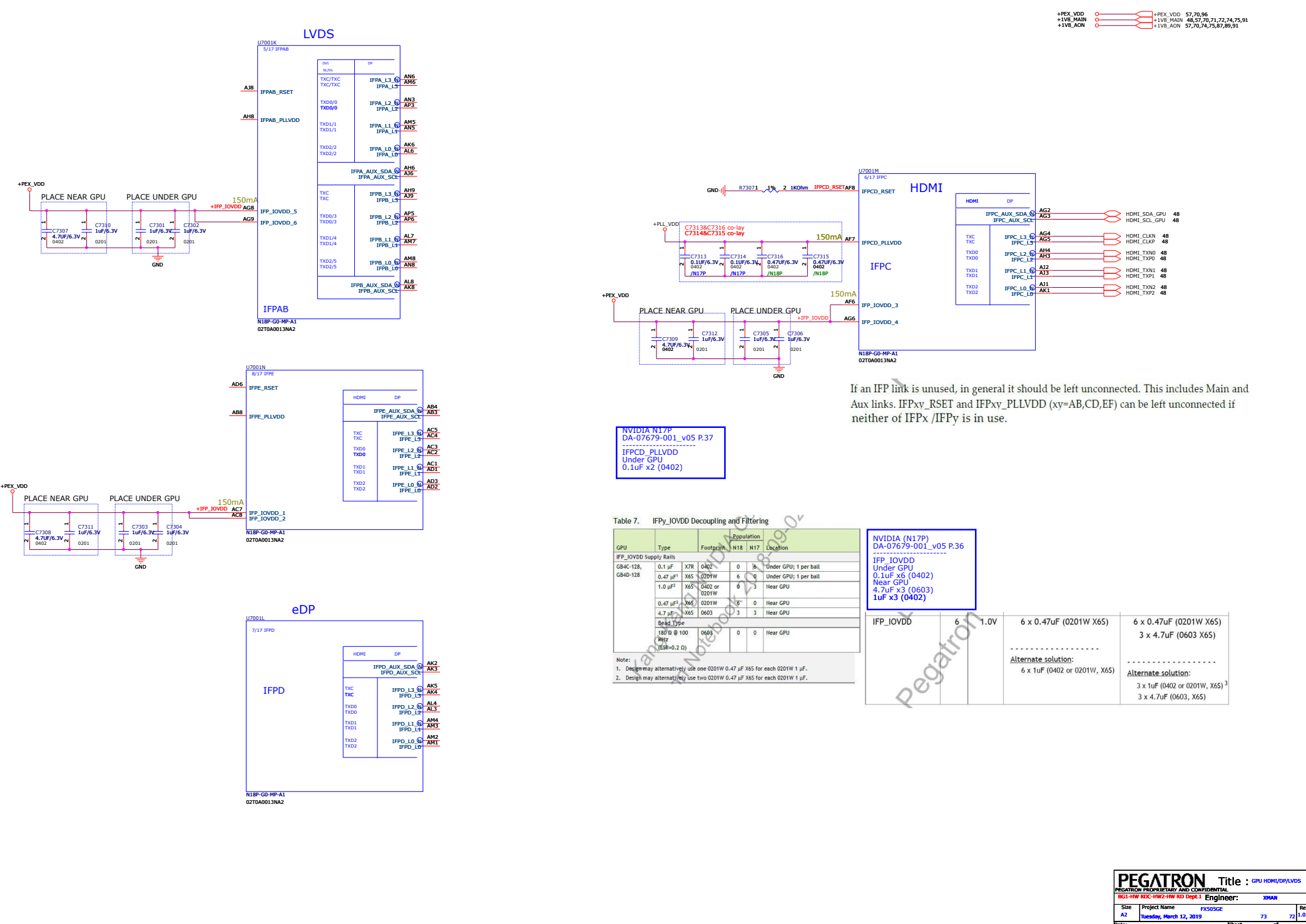
NVIDIA (N17P)  
DA-07679-001\_v05 P.38  
-----  
GPCPLL\_AVDD  
Under GPU  
0.1uF x1 (0402)  
Near GPU  
4.7uF x1 (0603)  
22 uF x1 (0805)



IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X6S, one per ball)	1 x 4.7uF (0603 X6S)
IFPCD_PLLVDD	1			1 x 22uF (0805 X6S)
IFPE_PLLVDD	1			1 x 30Ω bead (0603 max ESR 0.01 Ω)
GPCPLL_AVDDx	2		Alternate solution: 3 x 1uF (0402 or 0201W, X6S, one per ball)	
XSN_PLLVDD	2		2 x 0.47uF (0201W X6S)	
SP_PLLVDD	1		Alternate solution: 2 x 1uF (0402 or 0201W, X6S)	
VID_PLLVDD	1		1 x 0.47uF (0201W X6S)	
			Alternate solution: 1 x 1uF (0402 or 0201W, X6S)	
			Alternate solution: 1 x 0.47uF (0201W X6S)	
			Alternate solution: 1 x 1uF (0402 or 0201W, X6S)	

Part	Value	Unit	Qty	Location
IFPAB_PLLVDD	0.1 uF	X6S	1	Under GPU
IFPCD_PLLVDD	0.1 uF	X6S	1	Under GPU
IFPE_PLLVDD	0.1 uF	X6S	1	Under GPU
GPCPLL_AVDDx	0.1 uF	X6S	2	Under GPU
XSN_PLLVDD	0.1 uF	X6S	2	Under GPU
SP_PLLVDD	0.1 uF	X6S	1	Under GPU
VID_PLLVDD	0.1 uF	X6S	1	Under GPU
GPCPLL_AVDD	0.1 uF	X6S	1	Under GPU
IFPAB_PLLVDD	0.1 uF	X6S	1	Under GPU
IFPCD_PLLVDD	0.1 uF	X6S	1	Under GPU
IFPE_PLLVDD	0.1 uF	X6S	1	Under GPU
GPCPLL_AVDDx	0.1 uF	X6S	2	Under GPU
XSN_PLLVDD	0.1 uF	X6S	2	Under GPU
SP_PLLVDD	0.1 uF	X6S	1	Under GPU
VID_PLLVDD	0.1 uF	X6S	1	Under GPU
GPCPLL_AVDD	0.1 uF	X6S	1	Under GPU





+PEX\_VDD  
+1V8\_MAIN  
+1V8\_AON

+PEX\_VDD 57,70,96  
+1V8\_MAIN 48,57,70,71,72,74,75,91  
+1V8\_AON 57,70,74,75,87,89,91

If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy\_RSET and IFPxy\_PLLVDD (xy=AB,CD,EF) can be left unconnected if neither of IFPx /IFPy is in use.

NVIDIA N17P  
DA-07679-001\_v05 P.37  
-----  
IFPCD\_PLLVDD  
Under GPU  
0.1uF x2 (0402)

Table 7. IFPy\_IOVDD Decoupling and Filtering

GPU	Type	Footprint	Population		Location
			N18	N17	
IFP_IOVDD Supply Rails					
GB4C-128, GB4D-128	0.1 $\mu$ F	X78 0402	0	6	Under GPU; 1 per ball
	0.47 $\mu$ F <sup>1</sup>	X65 0201W	6	0	Under GPU; 1 per ball
	1.0 $\mu$ F <sup>2</sup>	X65 0402 or 0201W	0	3	Hear GPU
	0.47 $\mu$ F <sup>2</sup>	X65 0201W	5	0	Hear GPU
	4.7 $\mu$ F <sup>2</sup>	X65 0603	3	3	Hear GPU
	Board Type				
180 $\Omega$ @ 100 MHz (ESR<0.2 $\Omega$ )		0603	0	0	Hear GPU

Note:

- Design may alternatively use one 0201W 0.47  $\mu$ F X65 for each 0201W 1  $\mu$ F.
- Design may alternatively use two 0201W 0.47  $\mu$ F X65 for each 0201W 1  $\mu$ F.

NVIDIA (N17P)  
DA-07679-001\_v05 P.36  
-----  
IFP\_IOVDD  
Under GPU  
0.1uF x6 (0402)  
Near GPU  
4.7uF x3 (0603)  
1uF x3 (0402)

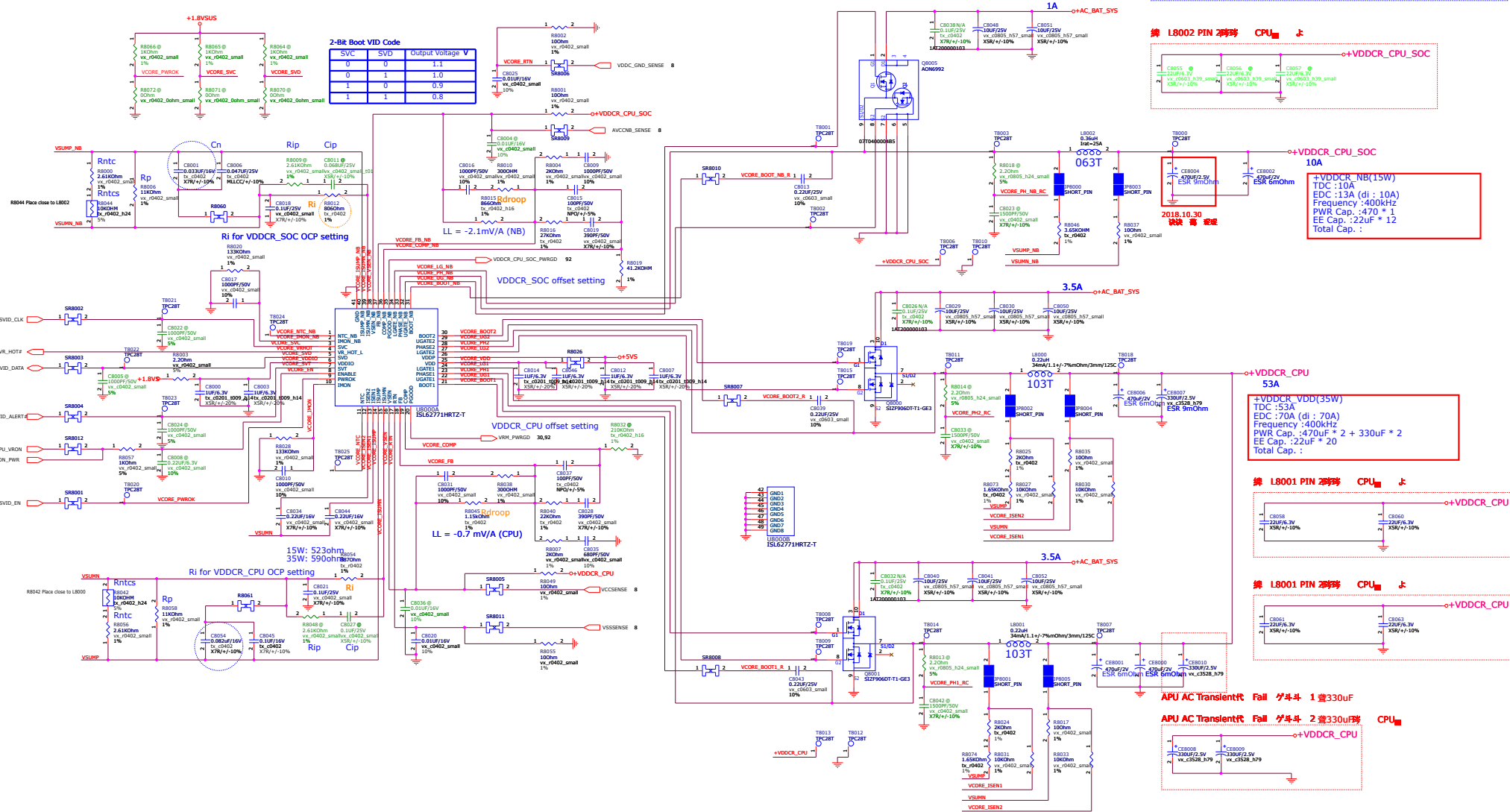
IFP_IOVDD	6	1.0V	6 x 0.47uF (0201W X65)	6 x 0.47uF (0201W X65) 3 x 4.7uF (0603 X65)
		Alternate solution:	6 x 1uF (0402 or 0201W, X65)	Alternate solution: 3 x 1uF (0402 or 0201W, X65) <sup>3</sup> 3 x 4.7uF (0603, X65)







## 35W VCORE POWER SUPPLY





# 5VO & 3VO POWER SUPPLY

Size Custom		Project Name FX505AN		Rev 1.0
Date: Tuesday, March 12, 2019		Sheet 81 of 97		

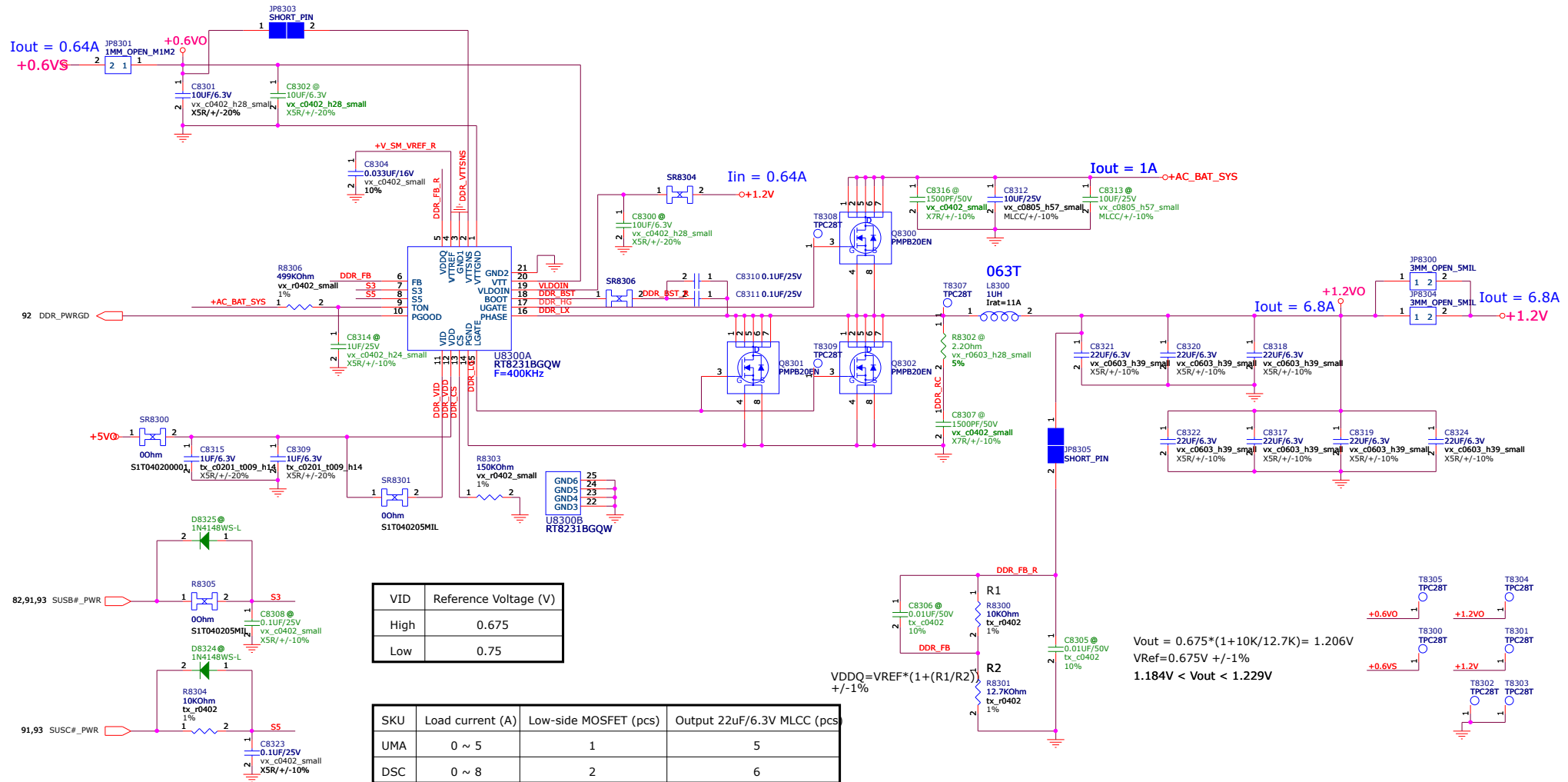


[illegible]

<b>PEGATRON</b>		Title : +0.9VS	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Wayne_Sung	
Size Custom	Project Name	FX505AN	Rev 1.0
Date: Tuesday, March 12, 2019	Sheet	82	of 97



# DDR & VTT POWER SUPPLY



<Variant Name>

**PEGATRON** Title :POWER\_DDR & VTT  
 PEGATRON PROPRIETARY AND CONFIDENTIAL

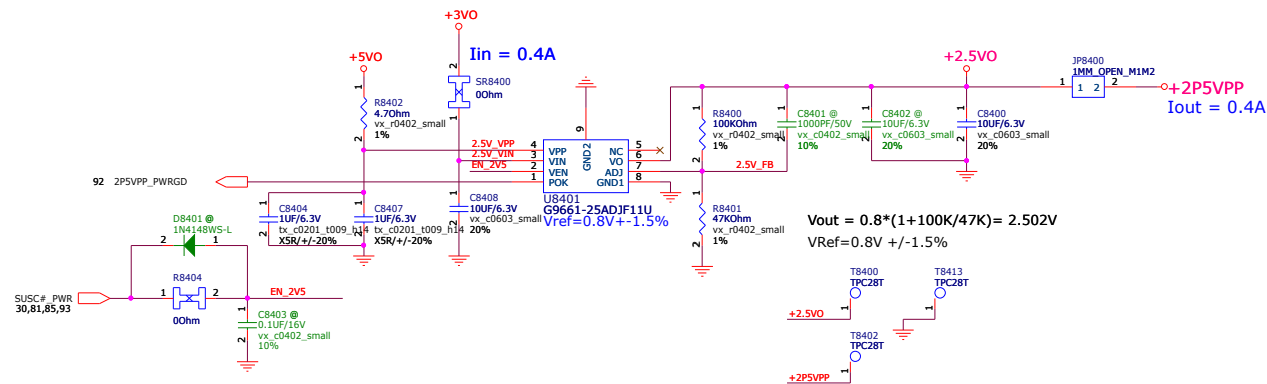
Engineer: **Wayne\_Sung**

Size: Custom Project Name: **FX505AN** Rev: 1.0

Date: Tuesday, March 12, 2019 Sheet 83 of 97

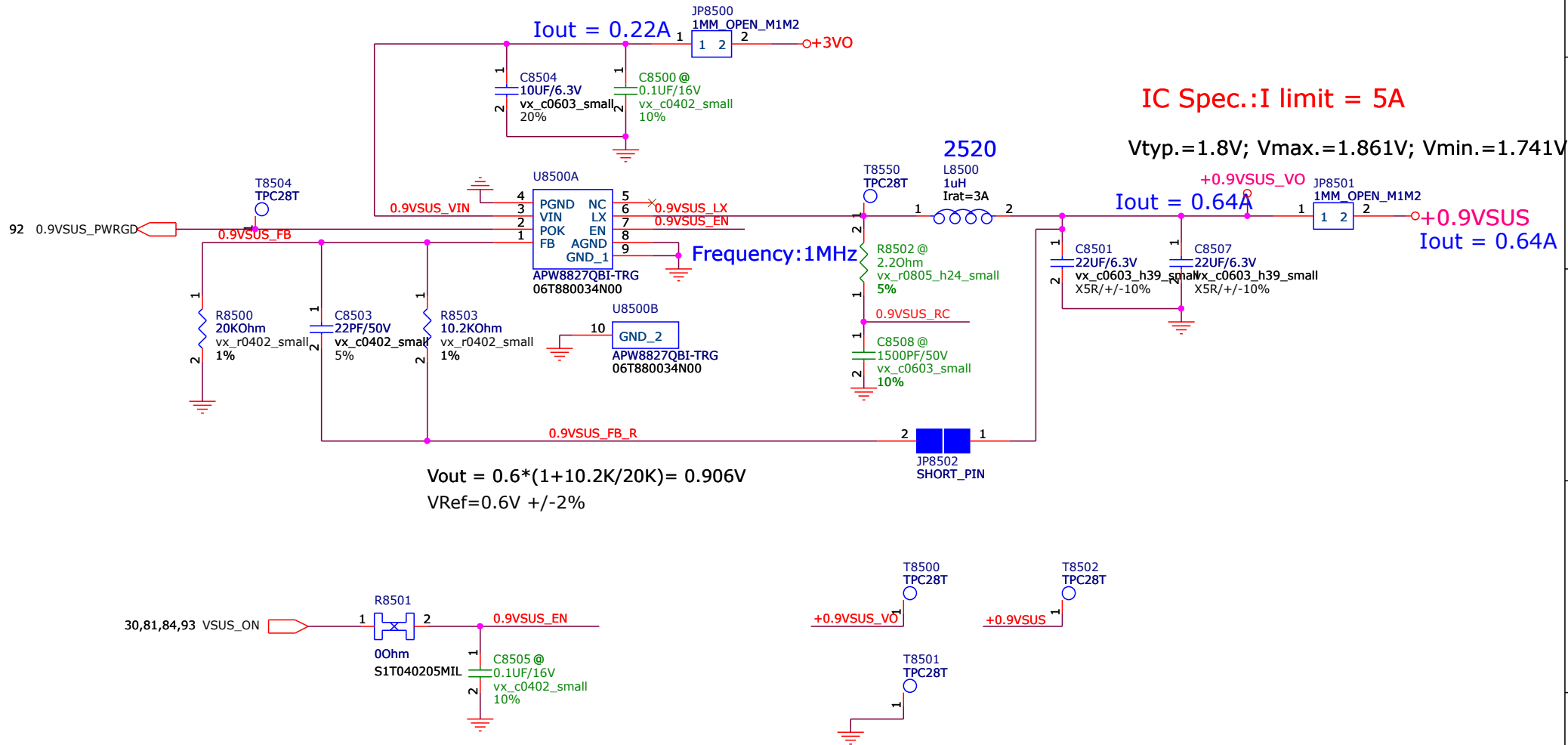


## 2.5V0 POWER SUPPLY





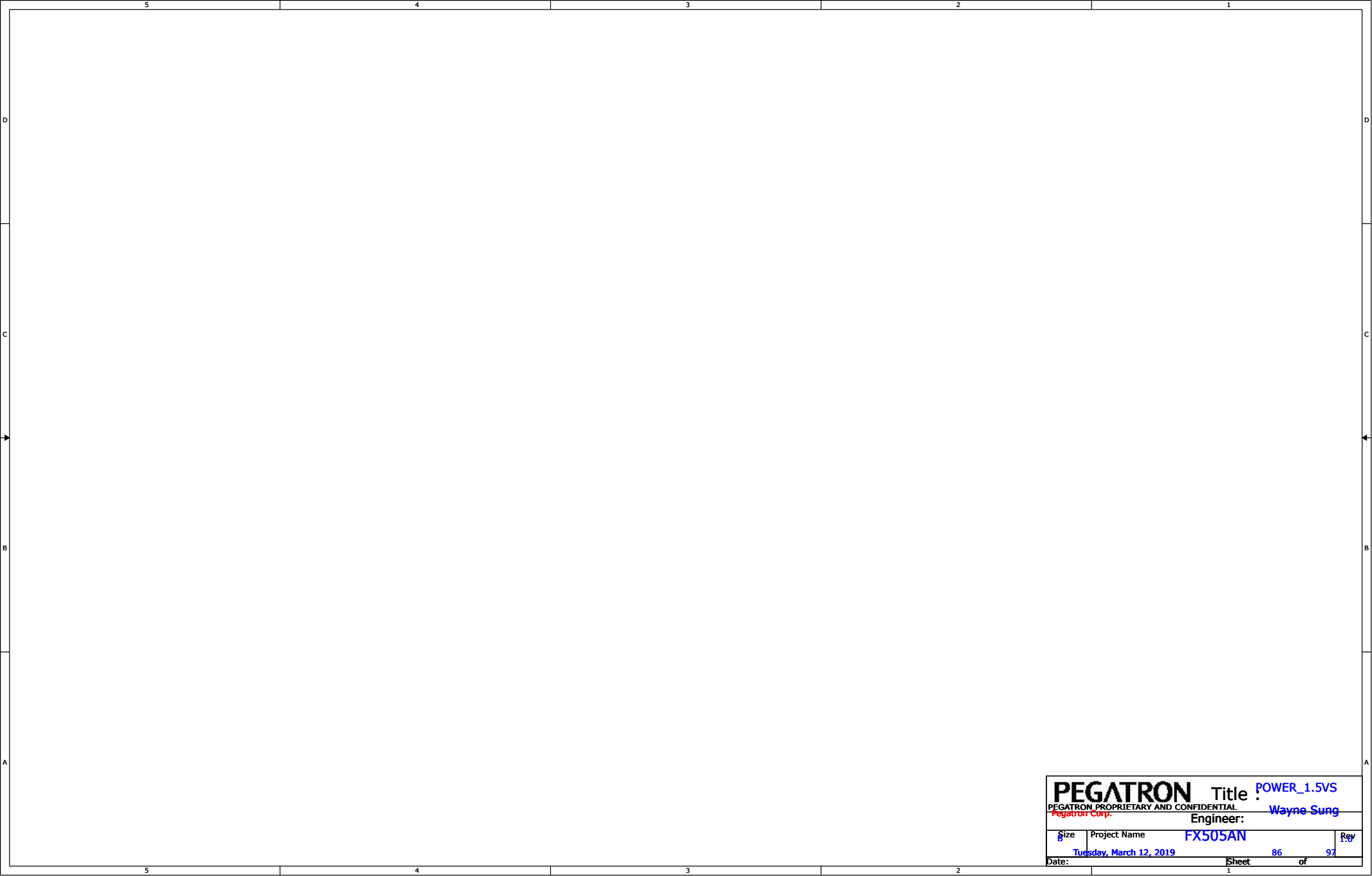
# 0.9VSUS POWER SUPPLY



<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_0.9VSUS</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer: <b>Wayne Sung</b>			
Size Custom	Project Name <b>FX505AN</b>		Rev 1.0
Date: <b>Tuesday, March 12, 2019</b>	Sheet	<b>85</b>	of <b>97</b>





Size

Project Name

FX505AN

Rev

97

Date:

Tuesday, March 12, 2019

Sheet

86

of

97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Pegatron Corp.

Title :

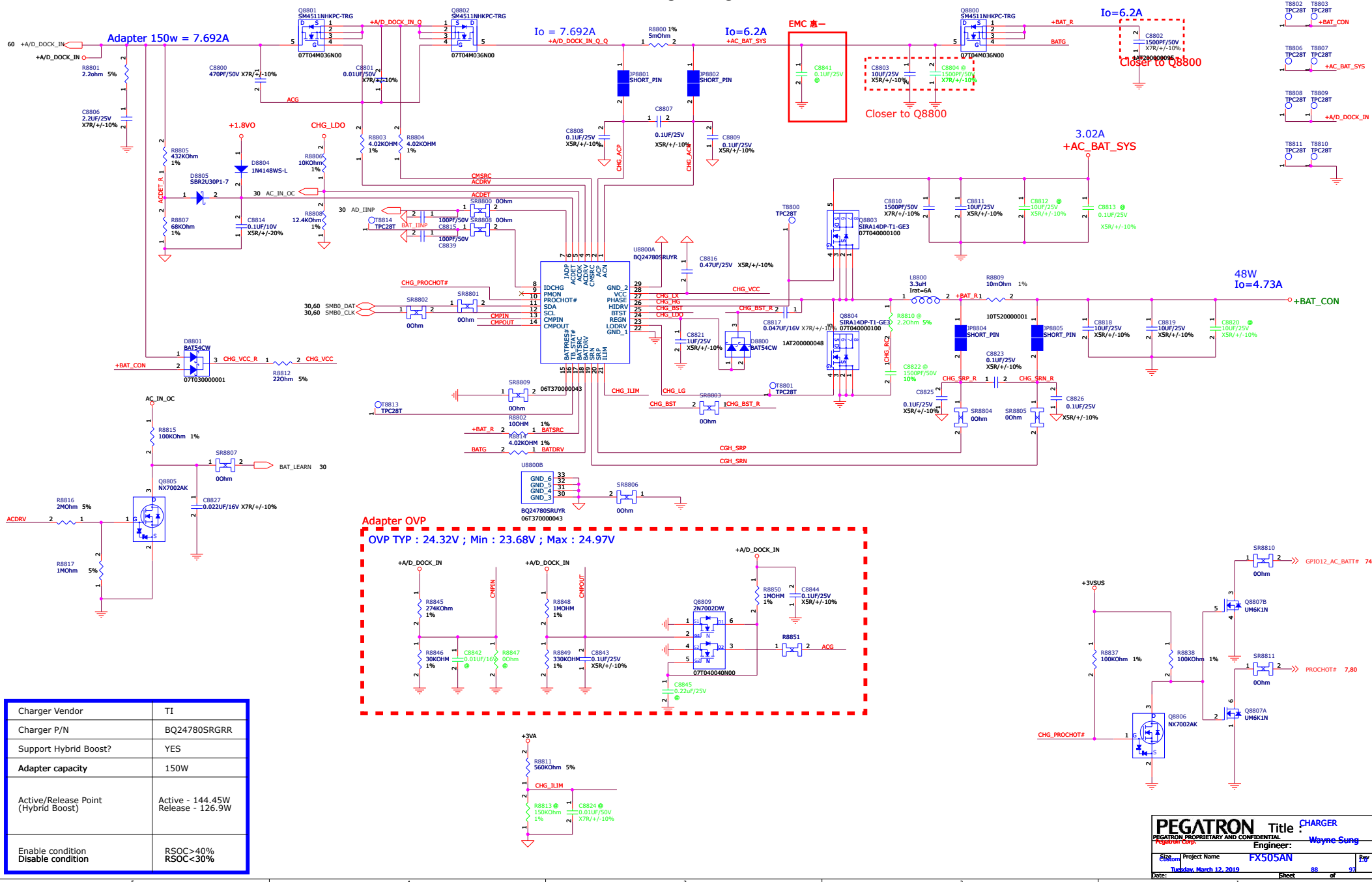
POWER\_1.5VS

Engineer:

Wayne Sung



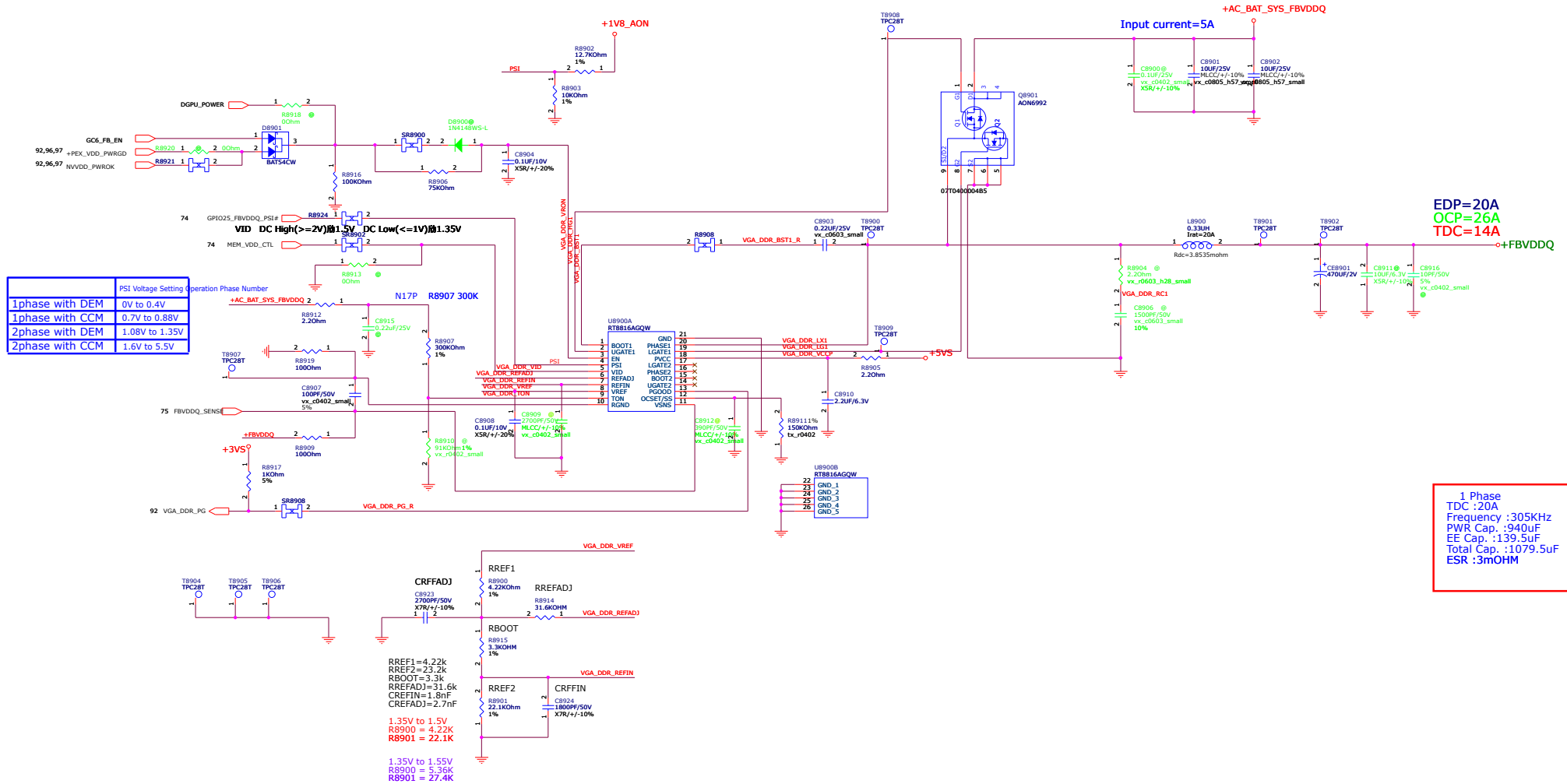
## BATTERY CHARGER



Charger Vendor	TI
Charger P/N	BQ24780SRGRR
Support Hybrid Boost?	YES
Adapter capacity	150W
Active/Release Point (Hybrid Boost)	Active - 144.45W Release - 126.9W
Enable condition Disable condition	RSOC>40% RSOC<30%



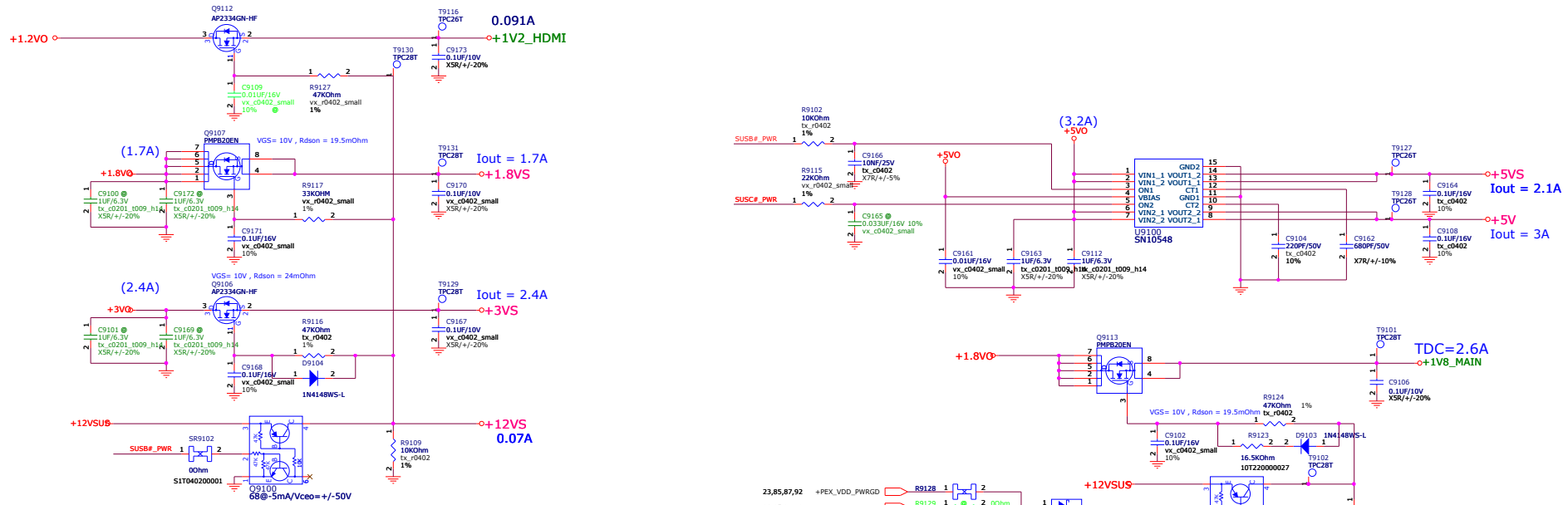
## +FBVDDQ POWER SUPPLY



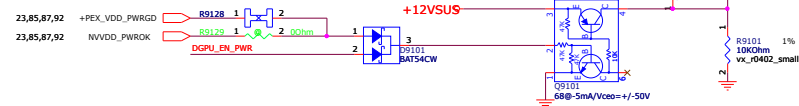
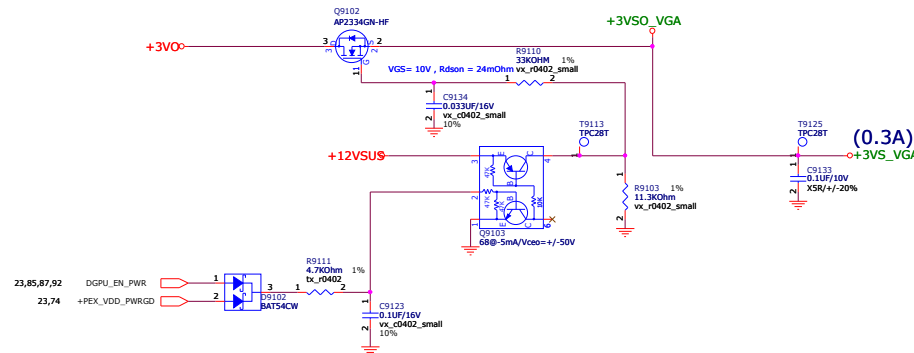
1 Phase  
TDC :20A  
Frequency :305KHz  
PWR Cap. :940uF  
EE Cap. :139.5uF  
Total Cap. :1079.5uF  
ESR :3mOHM



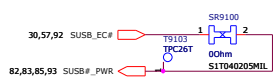
# LOAD SWITCH



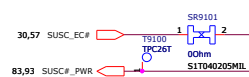
## DSC\_VGA\_PWR POWER



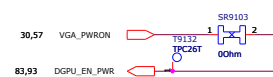
## SUSB#\_PWR POWER Control



## SUSC#\_PWR POWER Control

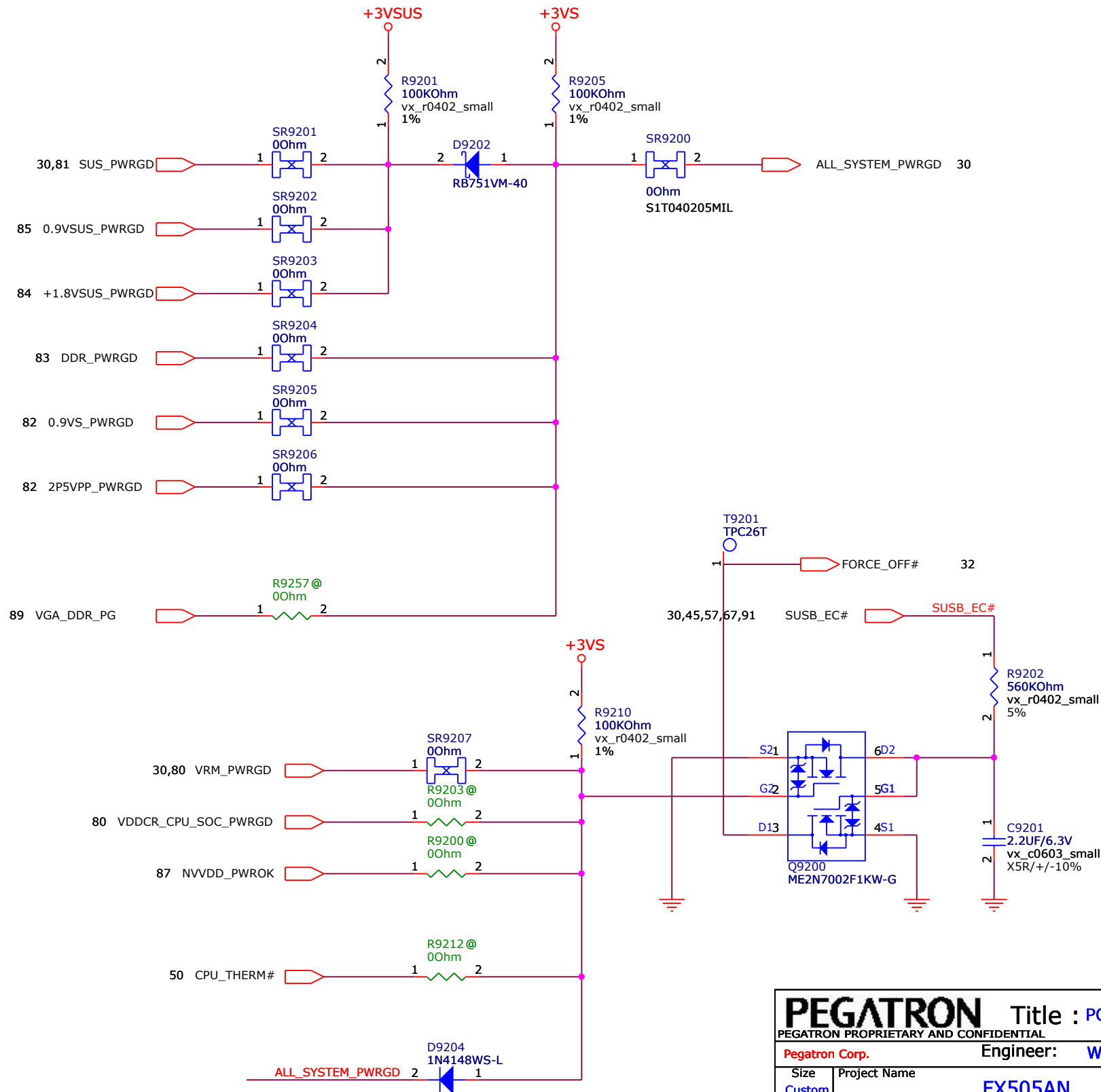


## DSC\_VGA\_PWR POWER Control





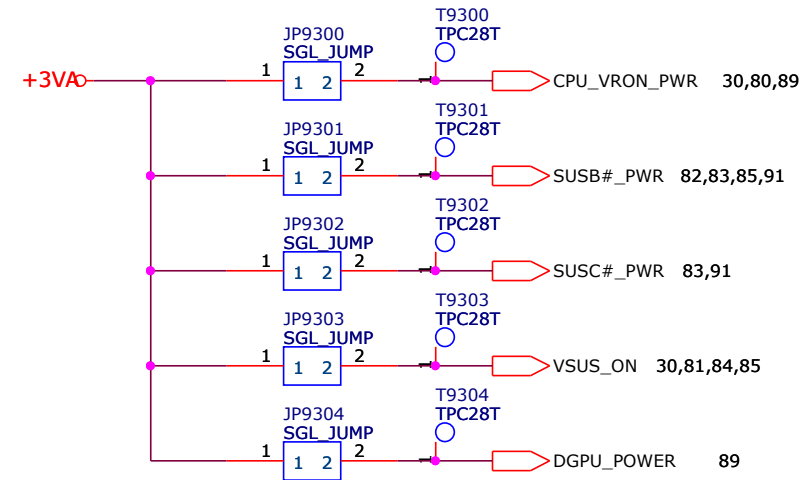
# POWER GOOD DETECTOR



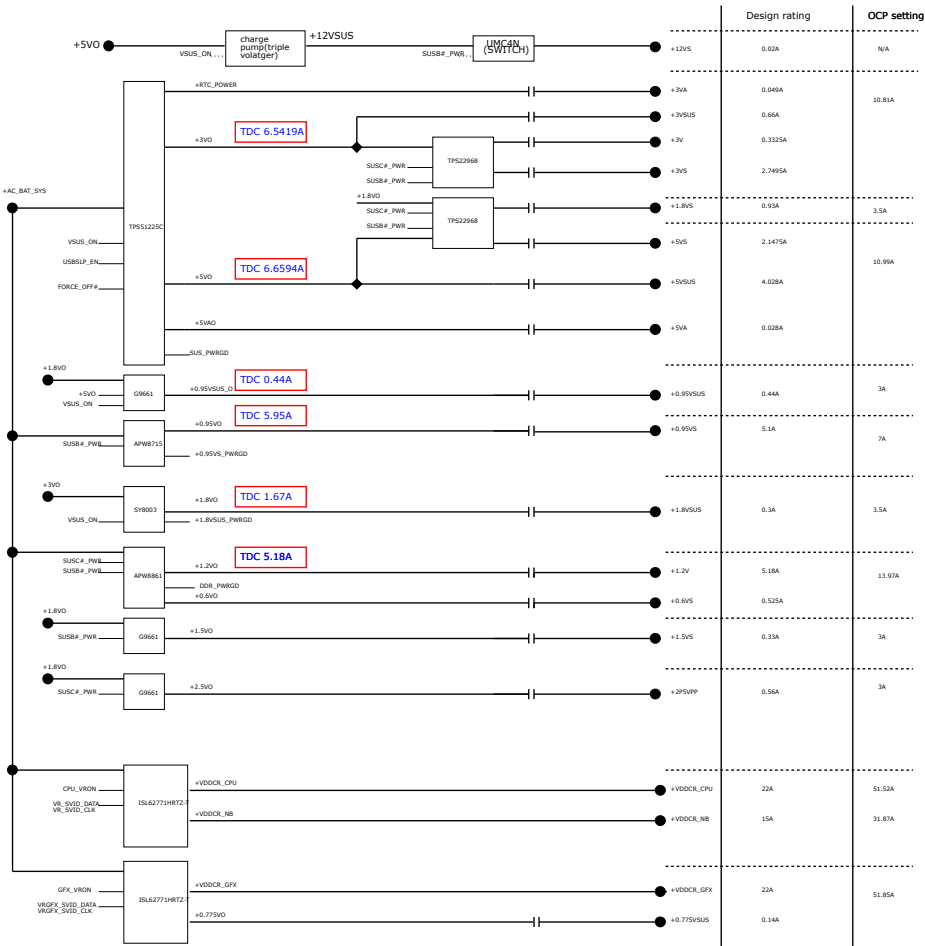


+AC_BAT_SYS	→	+AC_BAT_SYS	45,80,81,82,83,88,89
+BAT_CON	→	+BAT_CON	60,88
+RTC_POWER	→	+RTC_POWER	81
+5VA	→	+5VA	56,66,81
+3VA	→	+3VA	11,28,30,56,57,60,66,81,88
+5VO	→	+5VO	81,83,85,89,91
+3VO	→	+3VO	81,84,85,89,91
+2.5VO	→	+2.5VO	83
+1.8VO	→	+1.8VO	84,85,91
+1.8VO_VGA	→	+1.8VO_VGA	83
+1.2VO	→	+1.2VO	83
+0.9VO	→	+0.9VO	83
+0.9VSUS_VO	→	+0.9VSUS_VO	83
+0.6VO	→	+0.6VO	83
+12VSUS	→	+12VSUS	81,91
+5VSUS	→	+5VSUS	52,66,81
+3VSUS	→	+3VSUS	8,9,11,12,28,30,31,36,51,81,92
+1.8VSUS	→	+1.8VSUS	9,11,28,80,84,89
+0.9VSUS	→	+0.9VSUS	83
+12VS	→	+12VS	28,31,48,91
+5VS	→	+5VS	30,31,36,48,50,51,56,57,61,80,91
+3VS	→	+3VS	8,9,10,11,12,16,17,28,30,31,36,37,40,45,48,50,51,53,56,57,61,62,64,66,91,92
+1.8VS	→	+1.8VS	8,9,11,28,31,44,48,57,80,89,91
+0.6VS	→	+0.6VS	16,17,57,83
+3V	→	+3V	31,44,57,64,66,91
+1.2V	→	+1.2V	7,11,16,17,57,83
+2P5VPP	→	+2P5VPP	83
+1.8VS_VGA	→	+1.8VS_VGA	83
+1.35VS_VGA	→	+1.35VS_VGA	83
+VDDCI_VGA	→	+VDDCI_VGA	11,80,89
+VDDC_VGA	→	+VDDC_VGA	11,80,89
+VDDCR_CPU_SOC	→	+VDDCR_CPU_SOC	11,80
+VDDCR_CPU	→	+VDDCR_CPU	11,80

## FOR POWER TEST









92 + PEX\_VDD\_PWRGD

+3VS

+5V0

+1.2V0

1.3A

+1.0V\_VGA\_VPP

+1.0V\_VGA\_EN

+1.0V\_VGA\_FB

+1.0V\_VGA\_FB\_R

+1.0V\_VGA\_VO

1.3A

+PEX\_VDD

1.3A

R9616 10KOhm 1%

R9602 4.7Ohm 1%

R9600 11.8KOhm 1%

R9601 47KOhm 1%

C9602 2.2uF/6.3V X5R/+/-20%

C9601 10uF/6.3V X5R/+/-20%

C9603 100uF/50V X5R/+/-20%

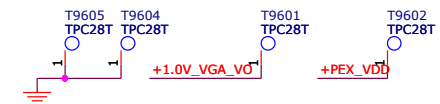
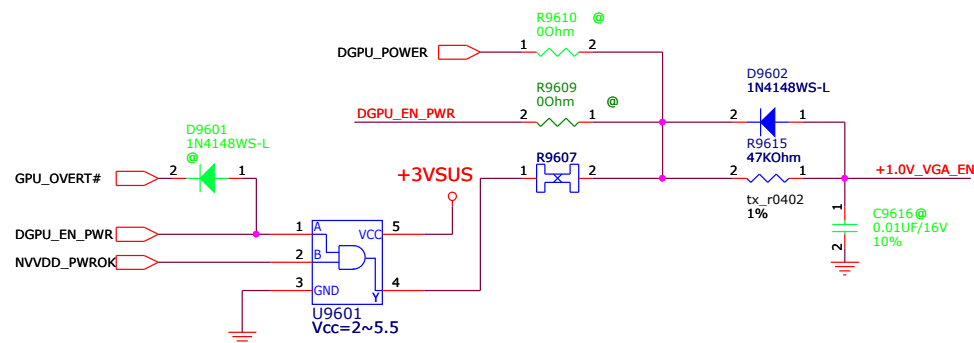
U9600 G9661-25ADJ1F11U Vref=0.8V +- 2%

JP9600 IMM\_OPEN\_M1M2

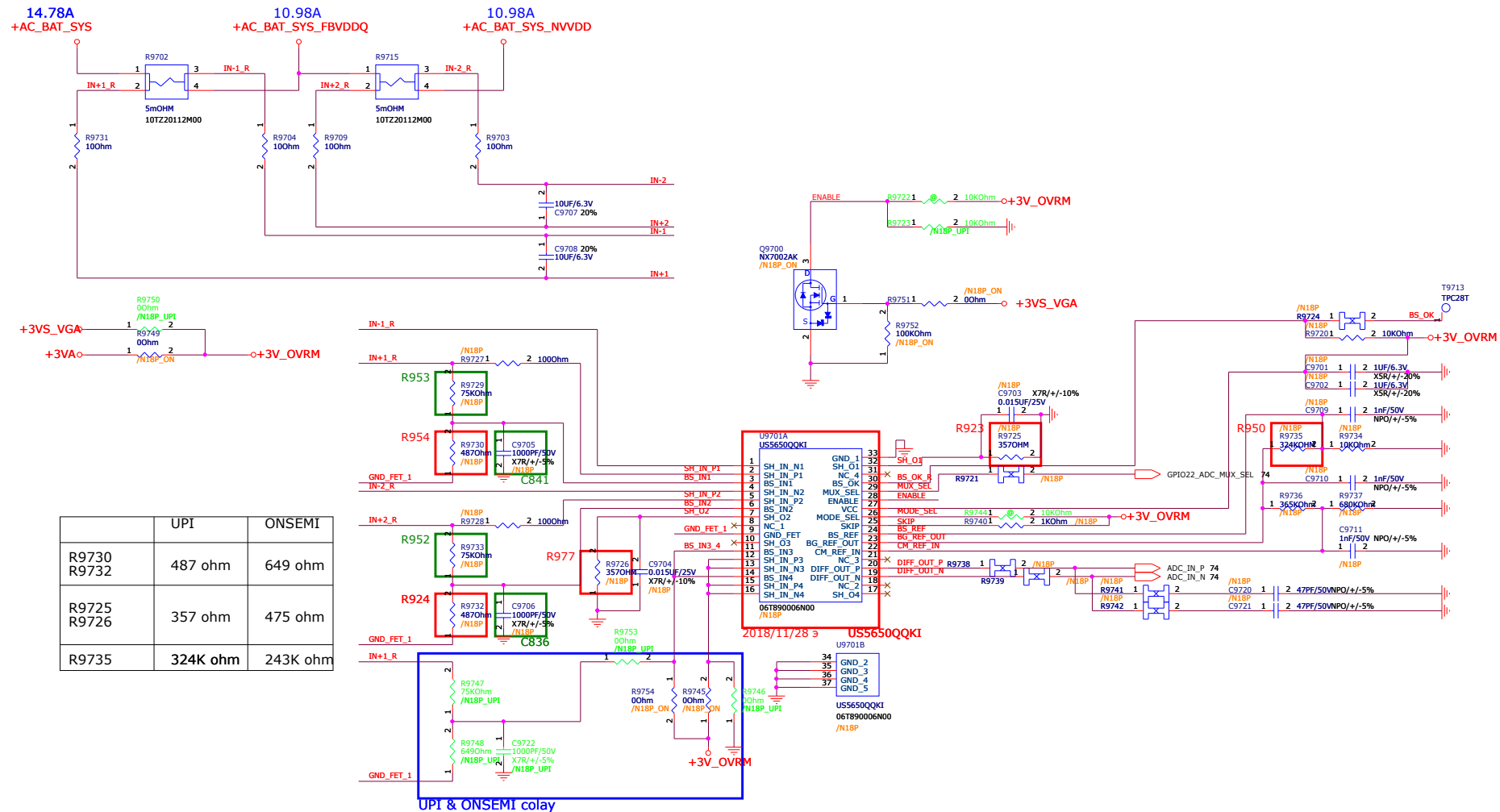
JP9601 SHORT\_PIN

92 + PEX\_VDD\_PWRGD

+PEX\_VDD  
MAX current : 1.3A  
PWR Cap. : 22uF  
Total Cap. : 22uF







	UPI	ONSEMI
R9730 R9732	487 ohm	649 ohm
R9725 R9726	357 ohm	475 ohm
R9735	324K ohm	243K ohm

Table 12. Power Monitoring with OnSemi OVR-M

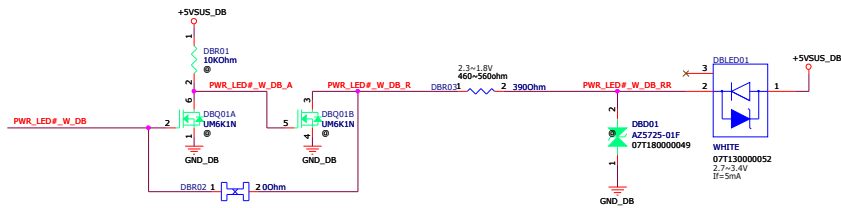
	Component Values				
GPU	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18P-G0	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF
N18P-G0					
MAX-Q					

Table 13. Power Monitoring with uPI OVR-M

	Component Values				
GPU	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18P-G0	487 Ω	357 Ω	324 kΩ	75 kΩ	1.0 nF
N18P-G0					
MAX-Q					

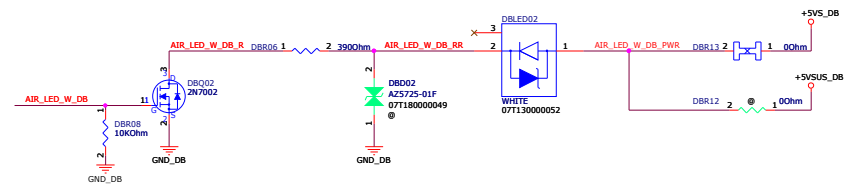


## Power LED

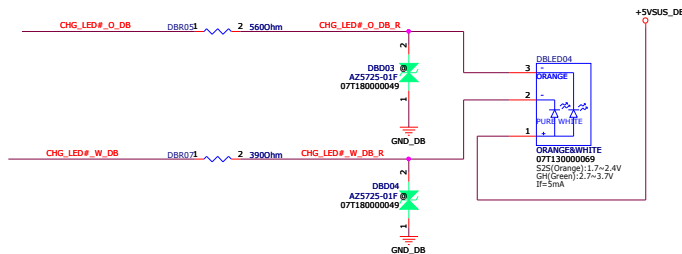


## AIR PLANE LED(White)

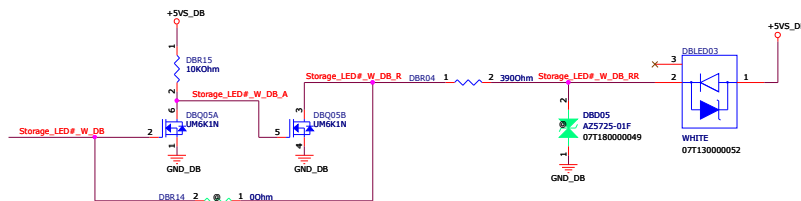
NOTE: AIR\_LED#\_R  
High -> airplane mode ON -> LED ON  
Low -> airplane mode OFF -> LED OFF



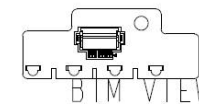
## Charger LED(White/Orange)



## HDD LED



## PCB/ID LOCATION

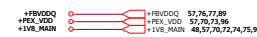


## Tooling Hole

PWR LED DBLED01  
Charger LED DBLED04  
HDD LED DBLED03  
RF LED DBLED02

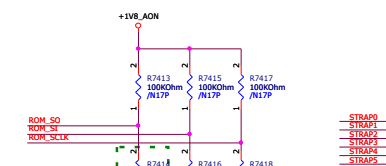
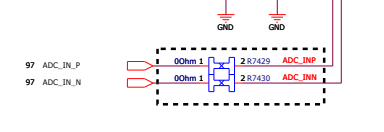
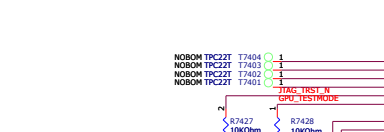
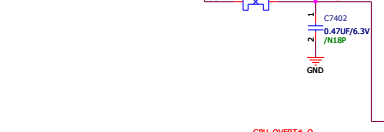
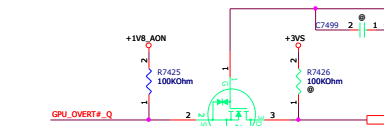
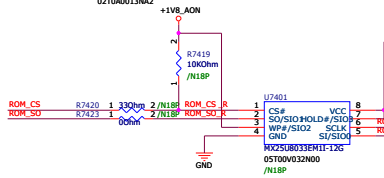
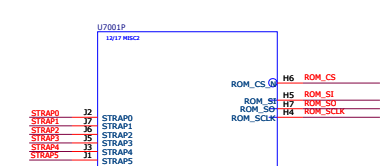
DBH01  
HOLE\_NPTH





<b>PEGATRON</b>		Title : GPU FB	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RDC-HW2-HW RD Dept.1		Engineer: XMAN	
Size	Project Name		Rev
Custom	FX505GE		1.0
Tuesday, March 12, 2019		71	72





For N18P 10KOhm RES

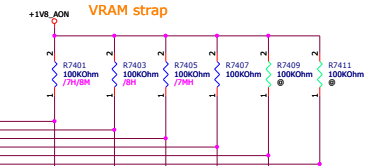
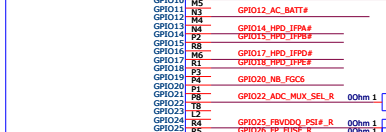
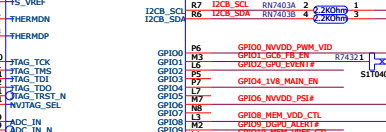
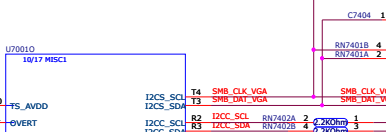
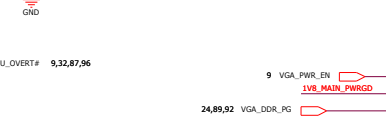
Peter : Refer to DA-07875-001\_v08 Table 5.4 & Table 5.5

Table 5.4 Display Link to SORX\_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	See This Row of Table 5.5
3	2	1
2	2	2
2	1	3
1	1	4
1	0	5

Table 5.5 RAMCFG Setting

Strap Pins	RAMCFG Setting
STRAP1	0 (0x000000)
STRAP2	1 (0x000001)
STRAP3	2 (0x000002)
STRAP4	3 (0x000003)
STRAP5	4 (0x000004)
STRAP6	5 (0x000005)



For N18P 10KOhm RES

Peter : Refer to DA-07875-001\_v08 Table 5.4 & Table 5.5

Table 5.4 Display Link to SORX\_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	See This Row of Table 5.5
3	2	1
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1	0	5

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STRAP6	5 (0x000005)

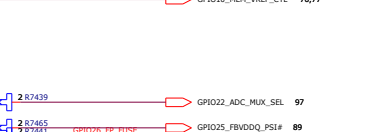
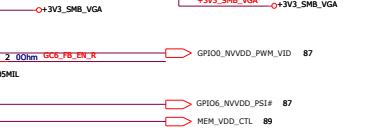
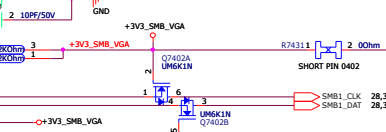
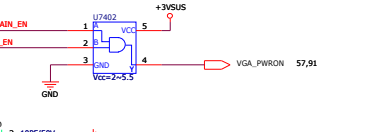
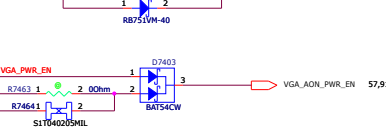


Table 4. N18P-GO GD08 Recommended Memories

Memory Density	Configuration	Manufacturer	Part Number	Die Size	Package	Speed	Max. Temp.	Status
1GB	1GB	Hynix	MT57LC5620F-08	8-die	QFP	1.0Gbps	105°C	Full Production
1GB	1GB	Samsung	K4G0320FC-08	8-die	QFP	1.0Gbps	105°C	Full Production

Table 5.3 RAMCFG Setting

Strap Pins	RAMCFG Setting
STRAP1	0 (0x000000)
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STRAP5	4 (0x000004)
STRAP6	5 (0x000005)

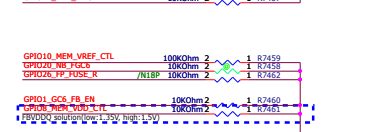
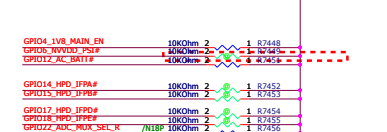
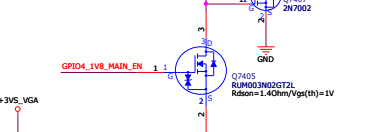
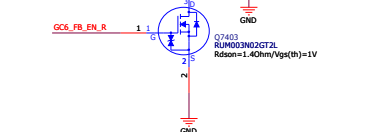
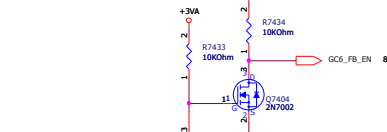
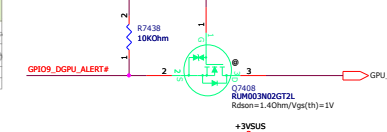


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STRAP4	3 (0x000003)
STRAP5	4 (0x000004)
STRAP6	5 (0x000005)

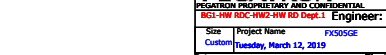
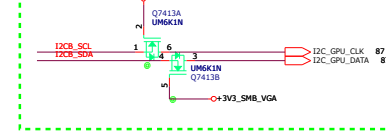
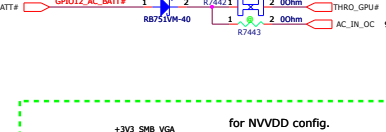
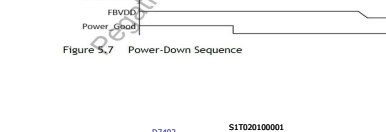
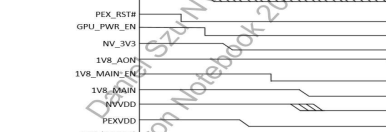
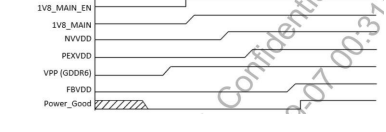
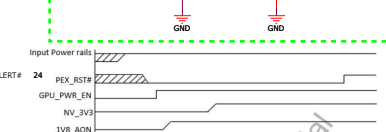


Table 4. N18P-GO GD08 Recommended Memories

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1GB	1GB	Hynix	MT57LC5620F-08	8-die	QFP	1.0Gbps	105°C	Full Production
1GB	1GB	Samsung	K4G0320FC-08	8-die	QFP	1.0Gbps	105°C	Full Production

Table 5.3 RAMCFG Setting

Strap Pins	RAMCFG Setting
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STRAP2	1 (0x000001)
STRAP3	2 (0x000002)
STRAP4	3 (0x000003)
STRAP5	4 (0x000004)
STRAP6	5 (0x000005)

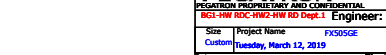
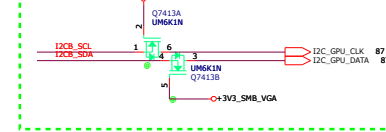
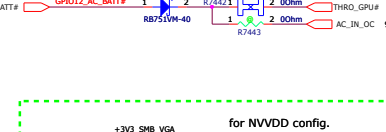
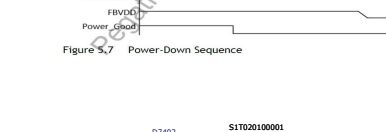
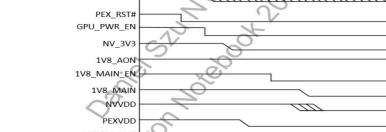
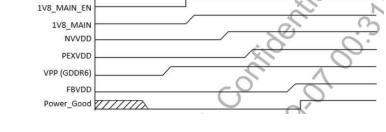
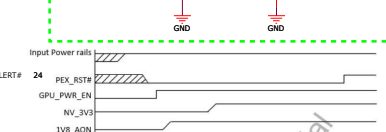


Table 4. N18P-GO GD08 Recommended Memories

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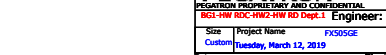
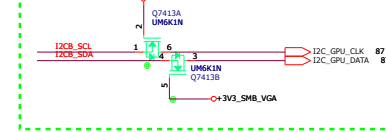
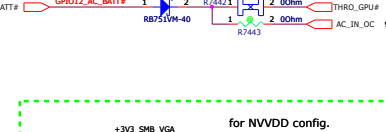
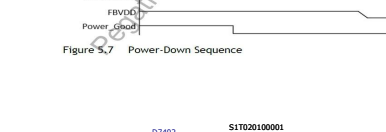
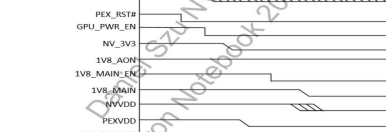
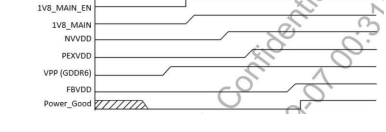
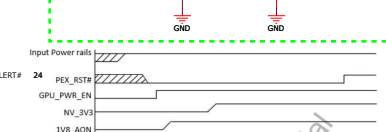


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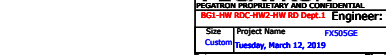
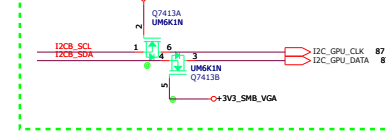
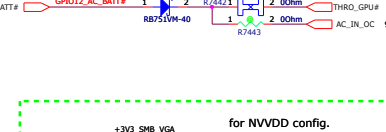
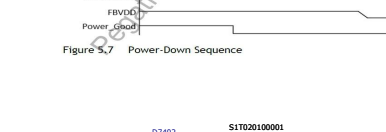
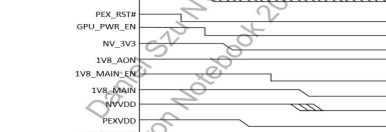
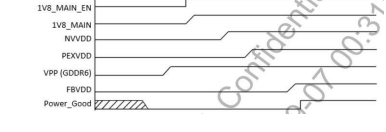
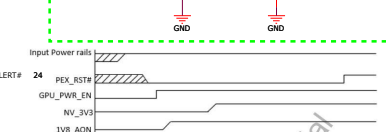


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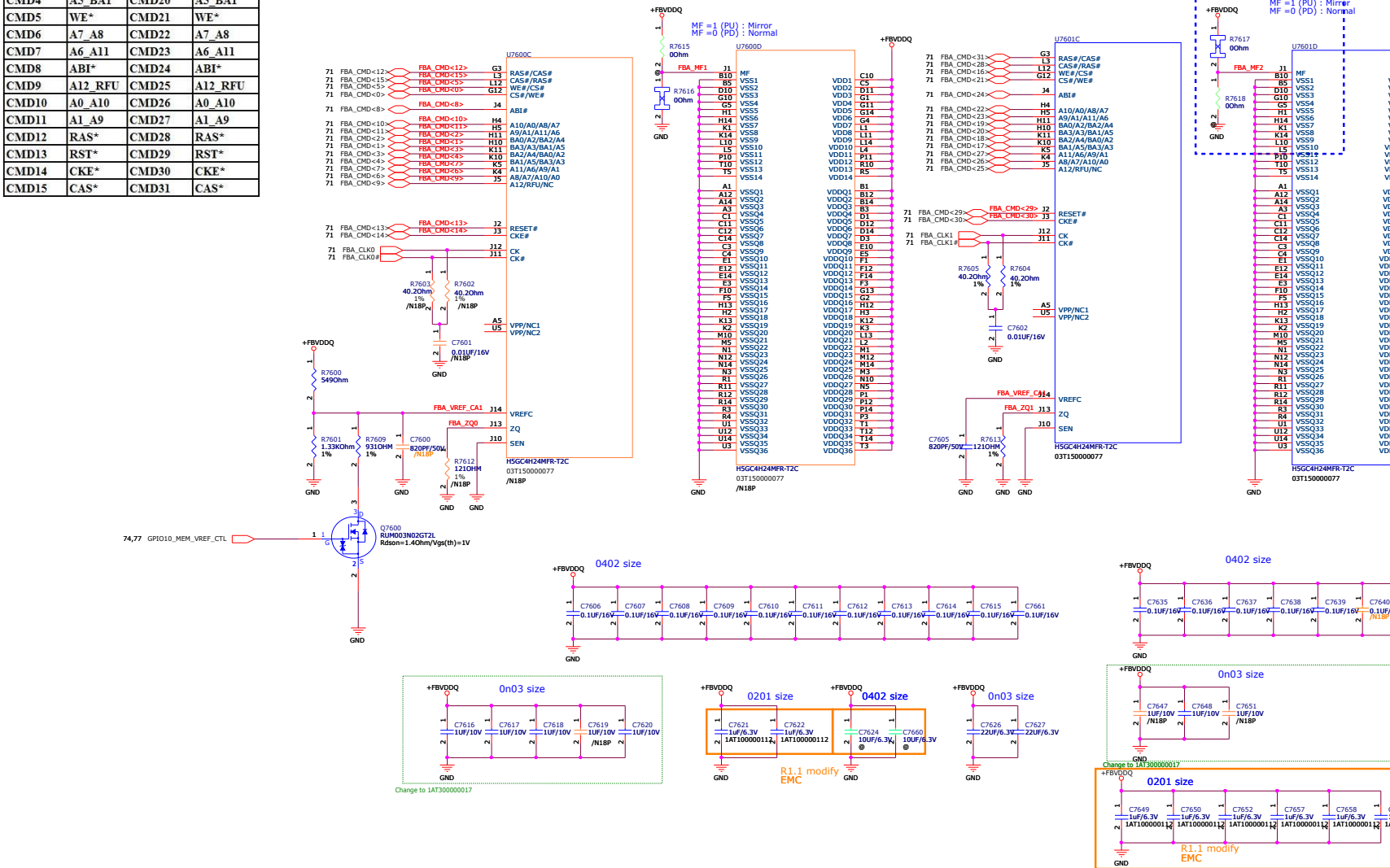




MEMORY : FBA Partition 31:0 (Normal)  
MEMORY : FBA Partition n3:32 (Mirror)

## GDDR5 Mode H Mapping

GB2B-64	Ch0 0..31	GB2B-64	Ch1 32..63
GB4B-128		GB4B-128	
GB4C-128		GB4C-128	
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*





叫牌U8700